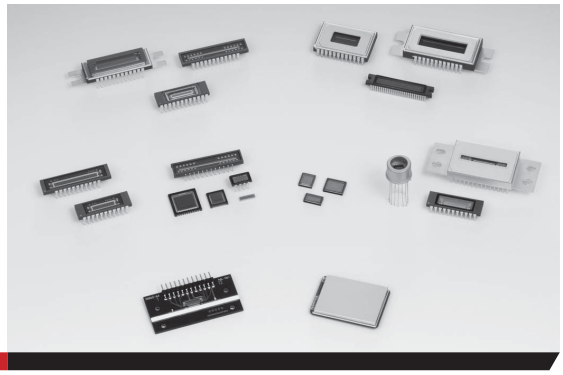
Image sensors

CHAPTER 05

Image sensors



For many years Hamamatsu has developed image sensors for measurement in broad wavelength and energy regions from infrared to visible light, to ultraviolet, vacuum ultraviolet, soft X-rays, and hard X-rays. We provide a wide range of image sensors for diverse applications and meticulously respond to customer needs such as for different window materials, filter combinations, and optical fiber couplings. We also supply driver circuits that are optimized for sensor evaluation or installation in equipment, as well as easy-to-use multichannel detector heads.

Back-thinned CCD image sensors are suitable for low-level light detection because of their high UV sensitivity, high S/N, and wide dynamic range. These sensors are extensively used in scientific and industrial fields such as DNA analysis, spectrophotometry, and semiconductor inspection systems, as well as in the medical field.

Front-illuminated CCD image sensors are used for imaging and measurement in the visible and near infrared region. Their applications have been recently expanded to include high-resolution X-ray imaging by coupling them to an FOP (fiber optic plate) with scintillator for use in medical equipment such as for dental diagnosis and in industrial non-destructive inspection.

NMOS linear image sensors are suitable for precision spectrophotometry because of their high UV sensitivity and superb linearity.

CMOS image sensors are well suited for industrial applications that require small, low-cost, and low-power consumption image sensors. Distance image sensors are CMOS image sensors that measure the distance to the target object using the TOF (time-of-flight) method. We also provide photodiode arrays with amplifiers, which have a unique hybrid structure comprised of a photodiode array with a freely changeable pitch and a CMOS amplifier array chip. These photodiode arrays serve as sensors for identifying paper money. When combined with a scintillator, these photodiode arrays are also used for non-destructive X-ray inspection of food and industrial materials.

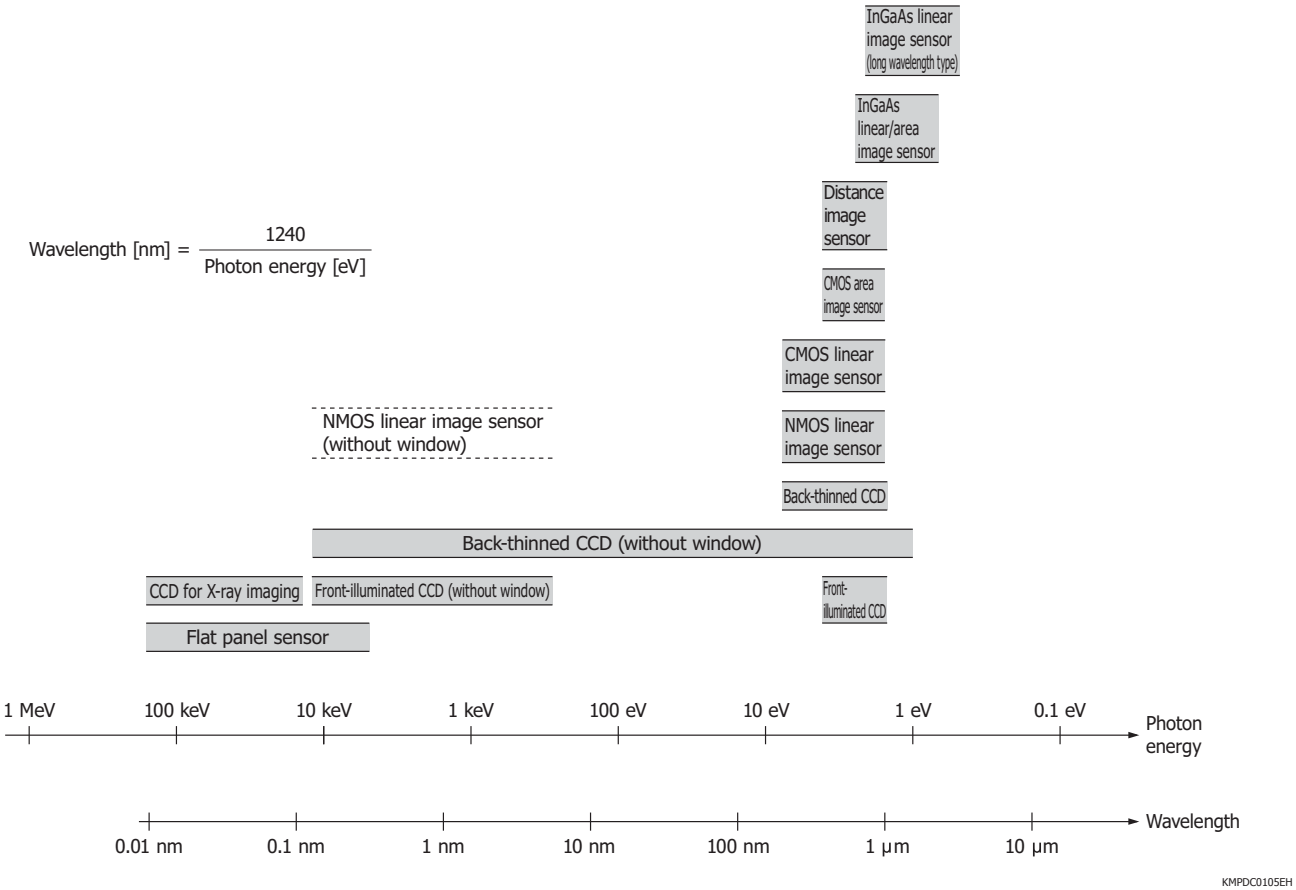
InGaAs image sensors consisting of an InGaAs photodiode array and CMOS charge amplifier array are used for near infrared spectrometry, DWDM monitoring, near infrared image detection, and the like.

Hamamatsu also provides flat panel sensors developed for X-ray detection, which combine a scintillator with a large-area CMOS image sensor made from monocrystalline silicon. (See Chapter 9, "X-ray detectors.")

Hamamatsu image sensors

Type	Features	Lineup
Back-thinned type CCD linear/area image sensor	Image sensors with high quantum efficiency from the visible region to the vacuum UV region	●For spectrophotometry ●For scientific measurements ●TDI-CCD area image sensor ●Fully-depleted area image sensor
Front-illuminated type CCD linear/area image sensor	Image sensors with low dark current and low noise	●For spectrophotometry ●For scientific measurements
NMOS linear image sensor	Image sensors with high UV sensitivity and excellent output linearity suitable for precision photometry	●Current output type (standard type) ●Current output type (infrared-enhanced type) ●Voltage output type
CMOS linear/area image sensor	Image sensors with internal signal processing circuits. These are suitable for applications that require low power consumption and device miniaturization.	●For spectrophotometry ●For industrial measurements
Distance linear/area image sensor	Sensors that measure the distance to the target object using the TOF method. Used in combination with a pulse modulated light source, these image sensors output phase difference information when light is emitted and received.	●Distance linear image sensor ●Distance area image sensor
Photodiode array with amplifier	Sensors combining a Si photodiode array and a signal processing IC. A long, narrow image sensor can also be configured by arranging multiple arrays in a row.	●Long and narrow type ●For non-destructive inspection
InGaAs linear/area image sensor	Image sensors for near infrared region. Easy handling due to built-in CMOS IC.	●For near infrared spectrophotometry ●For DWDM monitor ●For near infrared image detection
X-ray image sensor	Image sensor/photodiode arrays capable of acquiring high quality X-ray images when used in combination with an FOS (FOP with scintillator) or phosphor screen	●CCD/CMOS area image sensor for X-ray radiography ●TDI-CCD area image sensor ●Photodiode array with amplifier for non-destructive inspection
Flat panel sensor	Sensors for capturing X-ray images in real time	●For radiography ●For X-ray non-destructive inspection

Energy/spectral range detectable by image sensors (example)



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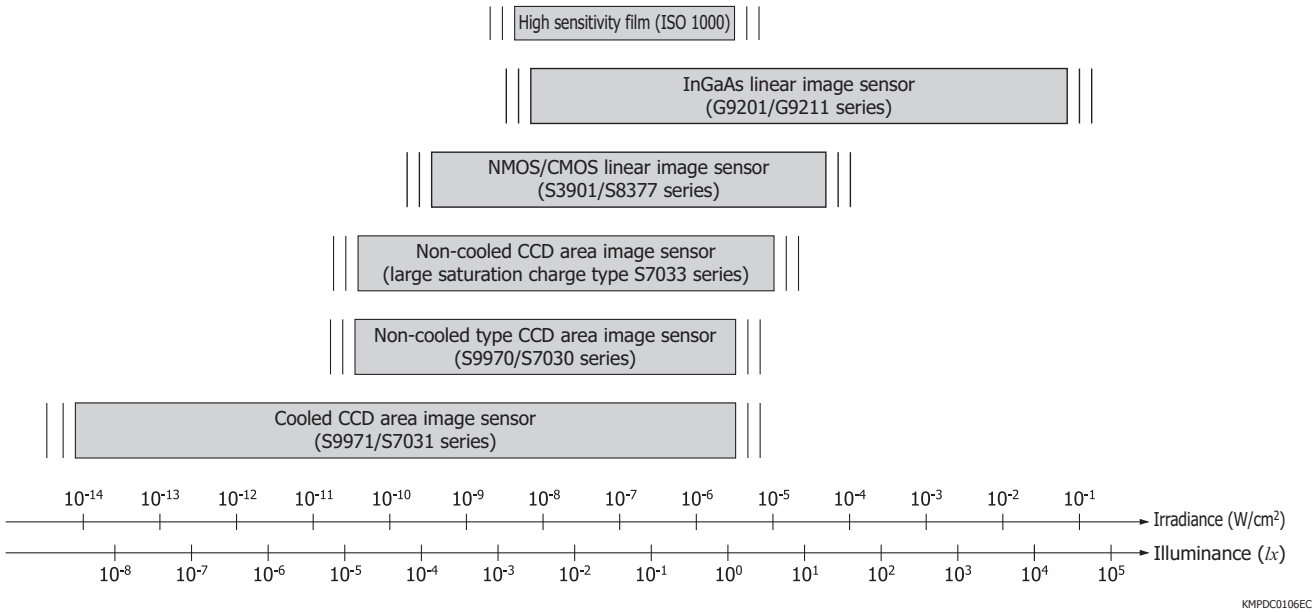
Light level range detectable by image sensors (example)



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1. CCD image sensors

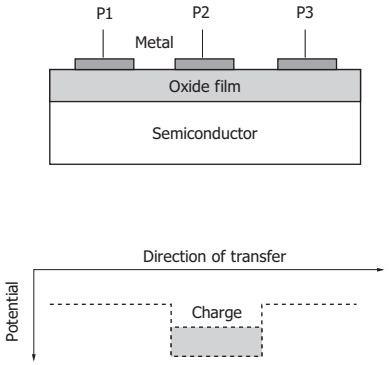
1 - 1 Structure and operating principle

CCD image sensors (referred to simply as CCD from now on) are semiconductor devices invented by Willard Boyle and George Smith at the AT&T Bell Laboratories in 1970. CCDs are image sensors grouped within a family of charge transfer devices (CTD) that transfer charges through the semiconductor by using potential wells. Most current CCDs have a buried channel CCD (BCCD) structure in which the charge transfer channels are embedded inside the substrate.

As shown in Figure 1-1, a CCD potential well is made by supplying one of multiple MOS (metal oxide semiconductor) structure electrodes with a voltage which is different from that supplied to the other electrodes. The signal charge packed in this potential well is sequentially transferred through the semiconductor toward the output section. Because of this, the CCD is also called an analog shift register.

CCDs are essentially semiconductor devices through which a signal charge is transferred. Currently, however, the term "CCD" has come to signify image sensors and video cameras since CCDs are widely used as image sensors.

[Figure 1-1] CCD basic structure and potential well



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CCD types

Currently used CCDs are grouped by their transfer method into the following five types.

- FT (frame transfer) type (two dimensional)
- FFT (full frame transfer) type (two dimensional)
- IT (interline transfer) type (two dimensional)
- FIT (frame interline transfer) type (two dimensional)
- One-dimensional type (linear image sensor)

Types except for the FFT and one-dimensional types are used in general-purpose video cameras. FFT and one-dimensional types are not suitable for use in video cameras because of their operating principle, and are mainly used in measurement and analysis applications.

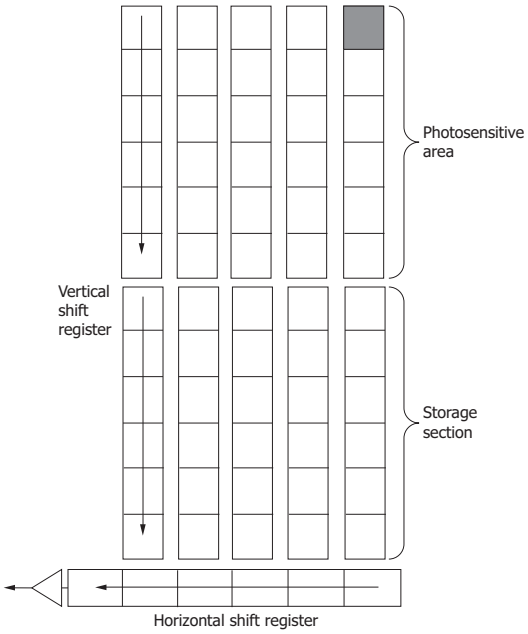
(1) FT type

The FT type CCD (FT-CCD) is comprised of two vertical shift registers for the photosensitive area and storage section, one horizontal shift register, and an output section. Vertical shift registers are also referred to as parallel registers, while the horizontal shift register is called the serial register or readout register. Transparent electrodes such as made from poly-silicon are generally employed as the electrodes for the photosensitive area.

When light comes through transparent electrodes into the CCD semiconductor, photoelectric conversion occurs and a signal charge is generated. This signal charge is collected into the potential well beneath the electrodes during a particular integration time. By utilizing the vertical blanking period, this signal charge is transferred at high speed to the storage section for each frame. Therefore in the FT type, the vertical shift register in the photosensitive area acts as a photoelectric converter device during the integration time.

The signal charge in the storage section is transferred to the output section through the horizontal shift register, while photoelectric conversion and signal accumulation take place in the photosensitive area. The signal charge is transferred to the horizontal shift register for each line in the storage section during the horizontal blanking period. In the FT type, all areas other than the photosensitive areas are covered with an opaque metal such as aluminum that prevents light from entering.

[Figure 1-2] Structure of FT type



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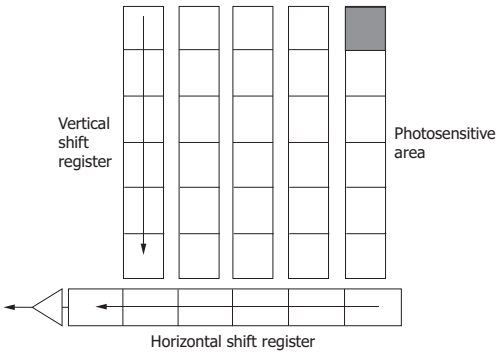
(2) FFT type

The FFT type CCD (FFT-CCD) basically has the same structure as the FT type except that there is no storage section. Because there is no storage section, the FFT type is usually used along with some type of external shutter mechanism. This limitation makes it difficult to use the FFT type in video cameras.

The operating principle of the FFT type is similar to that of the FT type. The signal charge is collected in a potential well in the photosensitive area during the integration time and then transferred to the output section via the horizontal shift register during the external shutter closed period and the like.
Since there is no storage section, the FFT type can be fabricated with a larger number of pixels or with a larger pixel size while using the same chip size, so the FFT type is mainly used for measurement camera systems with a slow frame rate. Most Hamamatsu CCDs are the FFT type.

[Figure 1-3] Structure of FFT type



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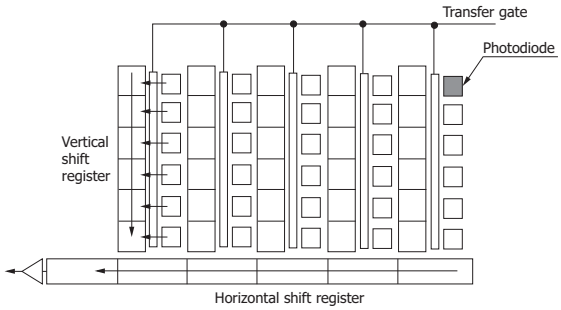
(3) IT type

The IT type CCD (IT-CCD) has an photosensitive area consisting of photodiodes or MOS structure diodes formed separately from the transfer section. Recent IT types use buried photodiodes with a low dark current. Vertical shift registers are arranged along photodiodes, and horizontal shift registers and output sections are also configured.
The signal charge produced by photoelectric conversion in a photodiode is stored in the junction capacitance of the photodiode itself and others. This charge is then transferred to the vertical shift register during the vertical blanking period through the transfer gate which is provided as a switch between the photodiode and the vertical shift register. This operation differs from the FT type in that the charge transfer from the photodiode to the vertical shift register is performed for all pixels simultaneously.
Subsequent operations are exactly the same as the FT type operation following "signal transfer to the storage section," so the signal charge is transferred to the horizontal shift register for every line during the horizontal blanking period.
Figure 1-4 shows a simplified structure of the IT type. As with the FT type, areas other than the photodiodes are light shielded with aluminum, etc. In the IT type, the signal charge is transferred from the storage section to the output section by using the period in which the charge is accumulated in the photodiode. This tends to cause a phenomenon called "smear" due to the signal charge leaking into the vertical shift register.

[Figure 1-4] Structure of IT type



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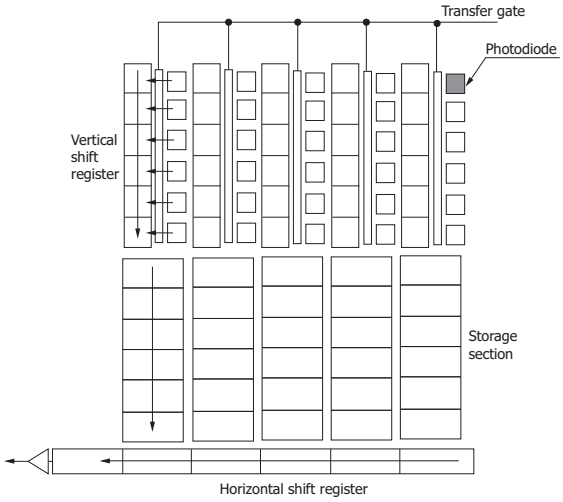
(4) FIT type

The FIT type CCD (FIT-CCD) was developed to solve the problems of the IT type CCD. The FIT type is configured basically by adding a storage section to the IT type. In the FIT type, as soon as a signal charge is transferred from the photodiodes to the vertical shift registers, the charge is transferred to the storage section at high speeds. The FIT type therefore ensures reduced smear compared to the IT type.

[Figure 1-5] Structure of FIT type



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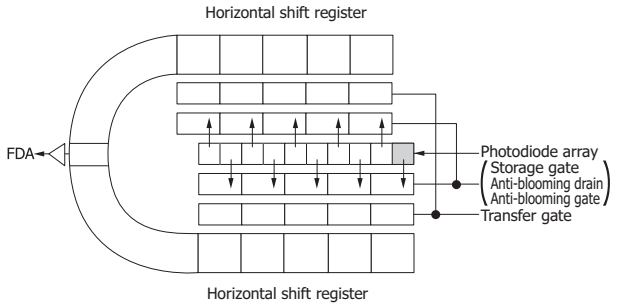
(5) One-dimensional type

In a one-dimensional type CCD, the signal charge generated by photoelectric conversion in a photodiode is collected in the adjacent storage gate. The signal charge is then transferred to the horizontal shift register through the transfer gate provided as a switch between the storage gate and the horizontal shift register. Charge transfer from the storage gate to the horizontal shift register is performed for all pixels simultaneously.
Figure 1-6 shows the structure of a one-dimensional type CCD. Signal charges from odd pixels in the photodiode array are transferred to the upper horizontal shift register, and signal charges from even pixels are transferred to the lower horizontal shift register. Those signal charges are alternately detected by a single FDA (floating diffusion amplifier, see "FDA" in section 1-1, "Structure and operating principle"). Transferring the odd pixel signal charges and even pixel signal charges to the separate horizontal shift registers makes it possible to fabricate a photodiode

array with a small pitch and to form anti-blooming and electronic shutter structures.

[Figure 1-6] Structure of one-dimensional type



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Charge transfer operation

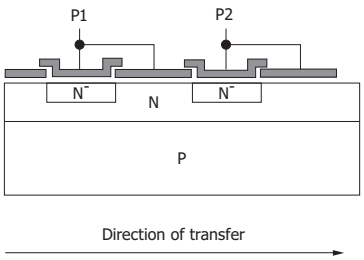
CCDs using two electrodes (gates) for one pixel are called 2-phase (drive) CCDs or 2-gate CCDs. Figure 1-7 shows the operating principle of a 2-phase CCD in which the signal charge is transferred by applying two clock pulses with different voltage levels (high level and low level).

In a 2-phase CCD, the signal charge is transferred in the direction determined by the difference in potential created in the semiconductor process. The signal charge is stored beneath the storage electrode. In Figure 1-7 for example, the signal charge is stored beneath the storage electrode for electrode P1 by setting electrode P1 to high level (setting electrode P2 to low level) at time t1.

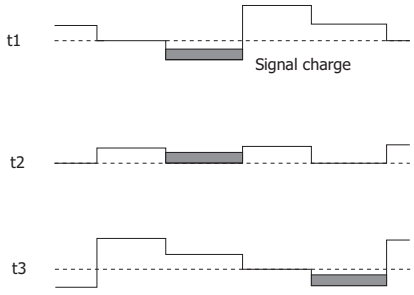
It is important in 2-phase CCDs to optimize the overlapping of clock pulses. As shown in the timing chart of Figure 1-7 (c), clock pulses must cross each other (at time t2) at a level higher than the midpoint of the high and low levels for P1 and P2 (for example, if the high level is V and the low level is 0, the cross point should be higher than V/2). The signal charges can be transferred by setting the clock phase so that P1 alternately goes high and low, while P2 goes low and high.

[Figure 1-7] Operating principle of 2-phase CCD

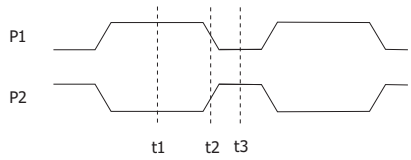
(a) Structure



(b) Potential



(c) Timing chart



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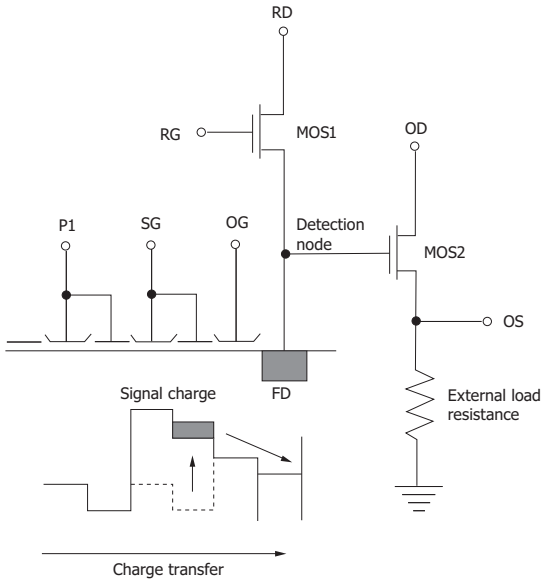
FDA

FDA (floating diffusion amplifier) is the most popular method for detecting the signal charge of a CCD. As shown in Figure 1-8, the FDA consists of a node for detecting charges and two MOSFETs (MOS1 for reset and MOS2 for charge-to-voltage conversion) connected to the node. The charge transferred to the detection node is converted into a voltage by MOS2 via the relation Q = CV. The detection node is reset by MOS1 to the reference level (voltage on RD) in order to read the next signal.

Noise accompanying the charge detection by FDA is determined by the capacitance of the node but can be almost entirely eliminated by CDS (correlated double sampling) invented by White.

The signal charge output timing is synchronized with the timing at which the summing gate (SG) goes from high level to low level, which is the last clock gate for the shift register.

[Figure 1-8] CCD output section using FDA



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Binning of signal charges

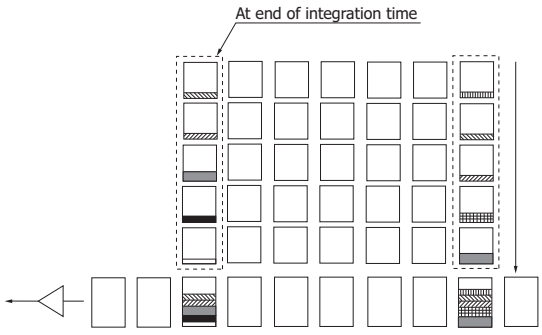
During CCD operation, a signal charge accumulates in the potential well of every pixel during the integration time. In FFT-CCDs, this means that the charge information is stored in two dimensions at the end of the integration time as shown in Figure 1-9 (a).
Since clock pulses can be input separately to the vertical shift register and horizontal shift register, an operation called "binning" can be performed. Binning is an operation unique to CCDs, and can be grouped into line (vertical) binning and pixel (horizontal) binning, depending on the direction that the signal charge is added.

(1) Line binning

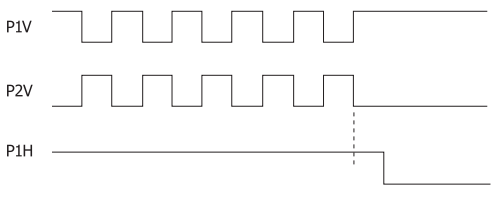
In line binning, the signal of each pixel is summed in the vertical direction. As shown in Figure 1-9 (b), the signal charge of each vertical pixel is sequentially transferred and added to one corresponding pixel of the horizontal shift register by applying a specified number of clock pulses P1V and P2V to the vertical shift register while the horizontal shift register clock pulse P1H is halted.
Line binning allows obtaining a signal which is equivalent to that obtained from a one-dimensional sensor having a very long photosensitive area in the vertical direction. Noise intrusion resulting from signal readout can be minimized since signal readout from the output section is performed at one time.

[Figure 1-9] Line binning

(a) Signal charge flow



(b) Timing chart



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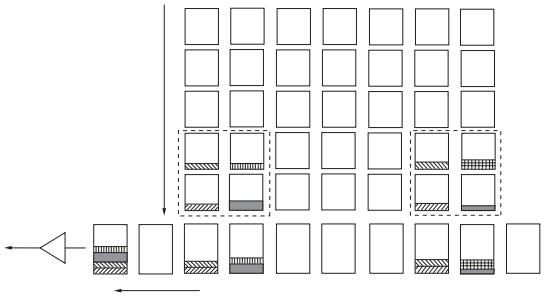
(2) Pixel binning

The last gate of the horizontal shift register in a CCD is an independent gate called the summing gate (SG). During operation not using pixel binning, the SG terminal is directly shorted to P2H (or the same clock pulses as P2H may be input to SG without shorting SG to P2H). Pixel binning can be performed by supplying a different clock pulse to SG.

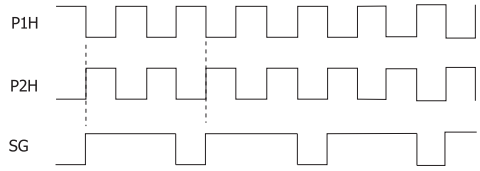
When used in combination with line binning, signals from 2 × 2 pixels for example can be summed as shown in Figure 1-10. In this case, the signals of two vertical lines are first summed by line binning into the pixels of the horizontal shift register. Next, in the signal charge readout by the horizontal shift register, the signals of the two horizontal pixels can be transferred and summed by applying just one clock pulse to the SG terminal during each period of two P1H clock pulses.
This method is effective in detecting low level light. For example, when the incident light level is too low to detect with a CCD having 1024 × 1024 pixels, operating it as a sensor having 512 × 512 pixels will acquire an image with higher contrast, although the spatial resolution will be lower.

[Figure 1-10] Pixel binning

(a) Signal charge flow



(b) Timing chart



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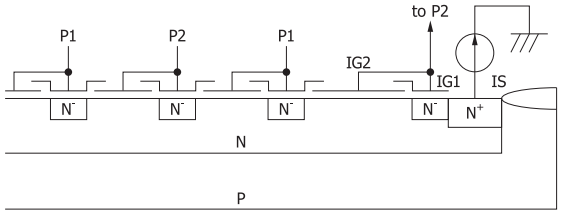
Signal charge injection

CCDs have input sources (ISV, ISH) and input gates (IGV, IGH) each arranged at the respective heads of the vertical shift register and horizontal shift register as the signal input terminals for electrical tests. In normal operation, a specified bias (see datasheets) should be applied to these test terminals. However, by applying a bias and clock pulses other than the specified values to these input sources and gates, a signal charge can be injected into the shift registers. This will reduce radiation-induced degradation of the CCD charge transfer efficiency. These terminals can also make quantitative evaluations of the saturation charge and the FDA linearity. A signal charge can also be injected into the shift registers by connecting a current source to the input sources and shorting the input gates to P2 for clock pulse input [Figure 1-11]. The charge injected by this method equals the product of the injection current value from the current source and the injection time (reciprocal of CCD drive frequency).

$$Qinj = Iinj \times t \cdots\cdots (1)$$

Qinj: injection charge [C]
Iinj : injection current [A]
t : injection time [s]

[Figure 1-11] Structure of signal charge injection section connected to current source



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Comparison with NMOS image sensor

The structure of CCD image sensors differs from NMOS image sensors, so their specifications and performance are also quite different from each other.

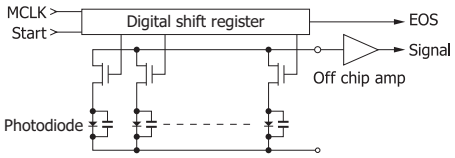
In NMOS image sensors, the signal charge accumulated in each photodiode is output to the signal line through a MOSFET switch by sequentially addressing the signal charge by a digital shift register. The operation at this point is performed by supplying TTL level clock pulses at a constant timing to the digital shift register, so that NMOS image sensors operate with just a single 5 V supply, except for the power to external signal processing sections.

On the other hand, CCD image sensors (IT type and one-dimensional type) transfer the signal charge accumulated in each photodiode to the analog shift register by turning on the MOSFET switch. The signal charge is then sequentially transferred by the analog shift register to the FDA in the final stage and is output. Operating a CCD image sensor requires more than one power supply, and the clock pulse amplitude must match the specified value. CCD image sensors exhibit a low readout noise level from a few to a dozen electrons (e^- rms). They also allow a high-speed readout at a pixel rate of 10 MHz or more depending on the amplifier bandwidth for the FDA.

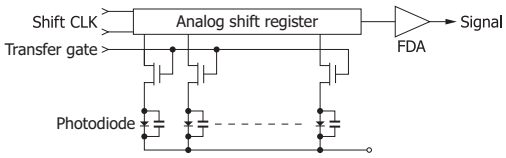
Although the noise level of NMOS image sensors runs as high as 3000 electrons (e^- rms), they can handle a signal charge over 100 times higher than CCD image sensors that typically handle several hundred thousand electrons. In general, if the light level to be detected is sufficiently high, using an NMOS image sensor is preferable because it simplifies the measurement system. In contrast, CCD image sensors have low noise and ensure an adequate S/N even at light levels that cannot be detected with NMOS image sensors. CCD image sensors are therefore suitable for low-light-level detection.

[Figure 1-12] Comparison of NMOS and CCD image sensors

(a) NMOS image sensor



(b) CCD image sensor (IT type and one-dimensional type)



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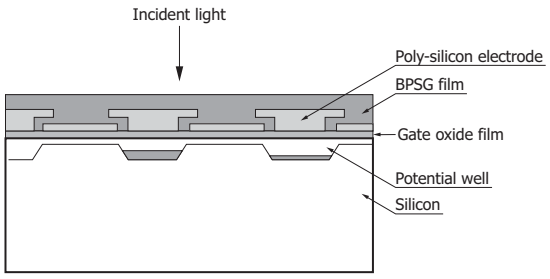
Front-illuminated type and back-thinned type

In general, CCDs are designed to receive light from the front side where circuit patterns are formed. This type of CCD is called the front-illuminated CCD. The light input surface of front-illuminated CCDs is formed on the front surface of the silicon substrate where a BPSG film, poly-silicon electrodes, and gate oxide film are deposited. Light entering the front surface is largely reflected away and absorbed by those components [Figure 1-13 (a)]. The quantum efficiency is therefore limited to approx. 40% at the highest in the visible region, and there is no sensitivity in the ultraviolet region.

Back-thinned CCDs were developed to solve such problems.[1)] Back-thinned CCDs also have a BPSG film, poly-silicon electrodes, and gate oxide film on the surface of the silicon substrate, but they receive light from the backside of the silicon substrate [Figure 1-13 (b)]. Because of this structure, back-thinned CCDs deliver high quantum efficiency over a wide spectral range. Besides having high sensitivity and low noise which are the intrinsic features of CCDs, back-thinned CCDs are also sensitive to electron beams, soft X-rays, ultraviolet, visible, and near infrared region.

[Figure 1-13] Schematic of CCDs

(a) Front-illuminated type



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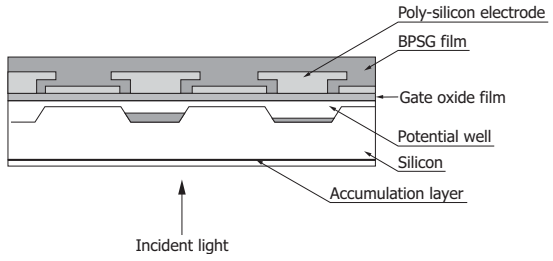
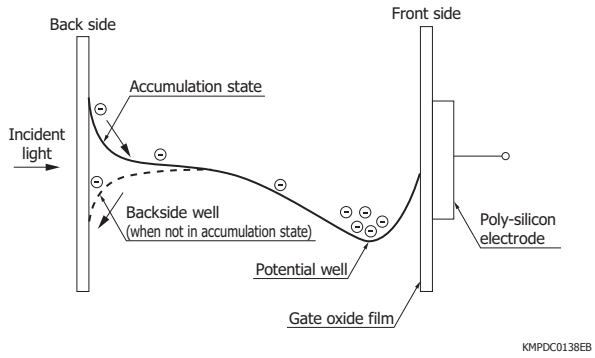
(b) Back-thinned type



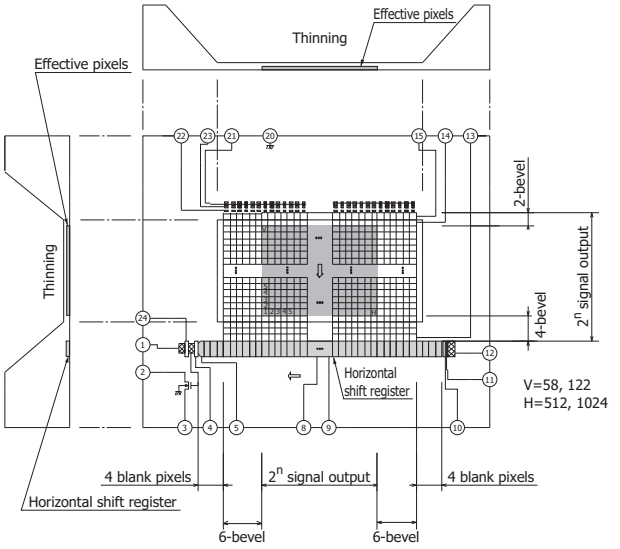
In order for back-thinned CCDs to achieve high sensitivity, it is essential to make the silicon substrate thin and to activate the photosensitive area. The photosensitive area is activated by forming an internal potential (accumulation) slope so that signal charges generated near the backside light input surface are smoothly carried to the CCD potential wells without recombining.[2) 3)] The internal potential in an accumulation state is shown in Figure 1-14.

[Figure 1-14] Internal potential of back-thinned CCD



When the back-thinned CCD is viewed from the light input side, the horizontal shift register is covered by the thick area of the silicon (insensitive area), and short-wavelength light hardly reaches the horizontal shift register. However, long-wavelength light may pass through the dead area of the silicon and may be received by the horizontal shift register.
If an external shutter is not used, light will enter the horizontal shift register during charge integration and transfer, and the false signal will be superimposed on top of the actual signal. For example, if a time invariant signal enters the horizontal shift register, a constant offset will be added to the signal. This effect will be smaller with shorter horizontal transfer time periods.
As necessary, use an external shutter, adjust the light input position, block the light, and take other effective measures.

[Figure 1-15] Device structure of back-thinned CCD (schematic of CCD chip as viewed from top of dimensional outline)



Near infrared-enhanced back-illuminated CCD

Normal back-thinned CCDs have high quantum efficiency in the ultraviolet to visible region. However, since the silicon substrate is about 15 to 30 µm thick, the quantum efficiency in the near infrared (NIR) region is low. For example, the quantum efficiency at a wavelength of 1 µm is approx. 20%. Thickening the silicon substrate improves sensitivity in the near infrared region, but the resolution decreases due to the charge diffusion in the neutral region (undepleted region).
Near infrared-enhanced back-illuminated CCDs were developed to solve such problems. To ensure high sensitivity in the near infrared region, the following two types are available.

(1) Fully-depleted type

Fully-depleted types use an ultra-high resistance N-type wafer to form a thick depletion layer. When the silicon resistivity is the same, the dopant concentration in N-type wafers can be reduced lower than that in P-type wafers, so the depletion layer can be thickened even when the same bias voltage is applied [Figure 1-16 (b)]. On the other hand, MPP operation (see “Dark current” in section 1-2, “Characteristics”) is not possible because the bias voltage is applied to the backside. Using a thick silicon substrate also causes the dark current to increase, so the CCD must be cooled to -70 to -100 °C. Since the silicon substrate for standard back-thinned CCDs is thin, it is difficult to fabricate large-area devices. However, fully-depleted back-illuminated CCDs use a silicon substrate whose thickness is about 100 to 300 µm over the entire area, so large-area devices can be easily fabricated.

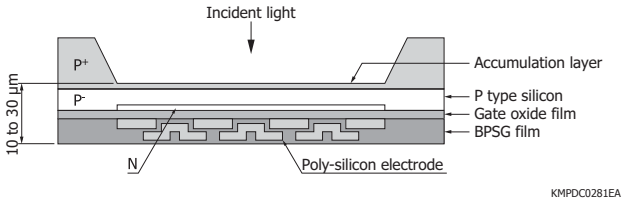
(2) Fine structure type

A special fine structure in the micron order is fabricated on the light input surface of the silicon [Figure 1-16 (c)].

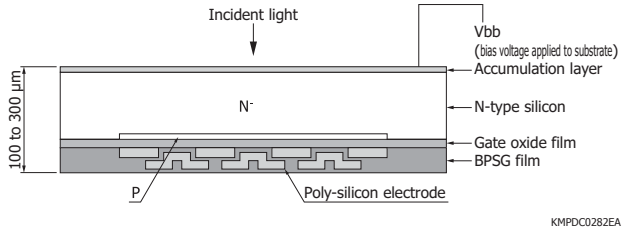
This structure traps in the silicon the near infrared light that would normally pass through the silicon to increase the absorption, which in turn achieves high CCD sensitivity. This also suppresses etaloning [Figure 1-51], which becomes a problem during the detection of near infrared light.

[Figure 1-16] Internal structure of back-illuminated CCD

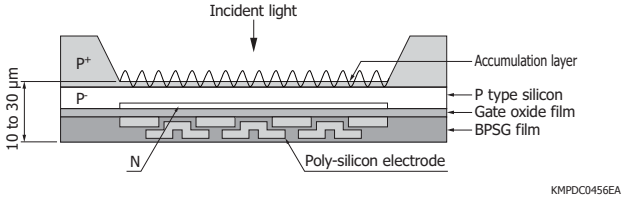
(a) Standard type



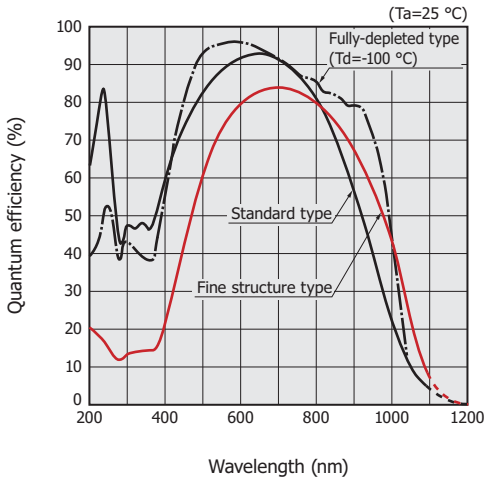
(b) Fully-depleted type



(c) Fine structure type



[Figure 1-17] Spectral response of back-illuminated CCDs (without window, typical example)



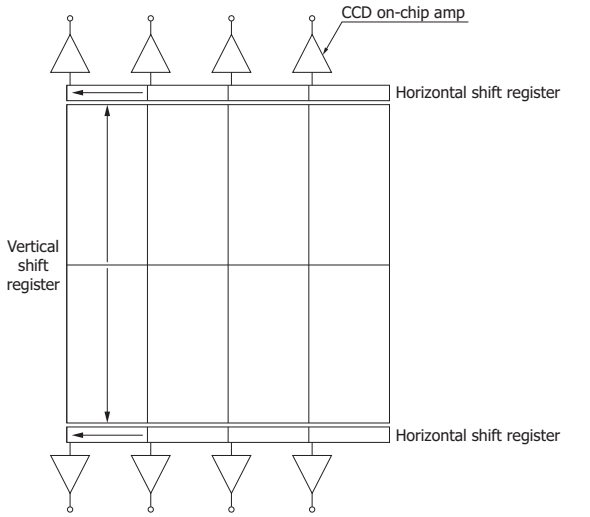
Multi-port CCD

The readout time of a CCD is determined by the number of pixels and readout frequency, and readout usually takes a long time. For example, when reading out signals from 1024 × 1024 pixels at a readout frequency of 100 kHz, the readout time will be 10 seconds or longer.

There is a trade-off between the readout frequency and readout noise. Increasing the readout frequency shortens the readout time but increases the readout noise [Figure 1-43].

Using multiple CCD amplifiers (multi-port configuration) allows parallel readout of pixels and improves the frame rate (number of frames acquired per second).

[Figure 1-18] Multi-port CCD structure



Thermoelectrically cooled CCD

CCD dark current varies with temperature; namely dark current is reduced by approx. one-half for every 5 to 7 °C decrease in temperature. As with MPP operation (see "Dark current" in section 1-2, "Characteristics"), cooling a CCD is an effective way to reduce the dark current and enhance the detection limit.

Thermoelectrically cooled CCDs contain a thermoelectric cooler (Peltier element) in the package, which efficiently cools the CCD. The cooling temperature is determined by maximum heat absorption and heat dissipation capacities of the thermoelectric cooler. The following parameters differ depending on the thermoelectric cooler.

· Maximum current (Imax)
· Maximum voltage (Vmax)
· Maximum heat absorption (Qmax)

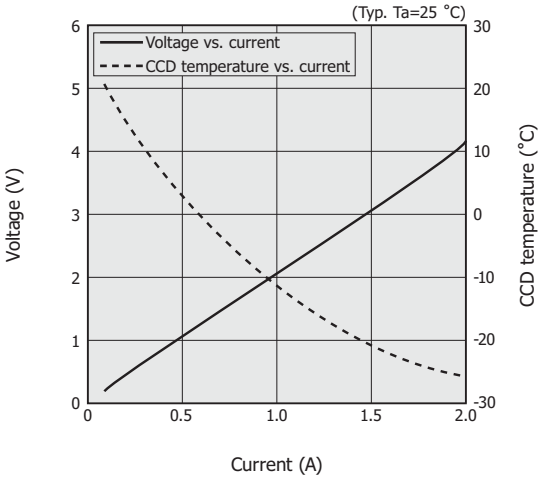
To avoid damaging a thermoelectric cooler and CCD, always operate them within the ratings specified in the datasheets. Heat dissipation methods are important when using a thermoelectric cooler. The cooling might be inadequate unless the heat is sufficiently dissipated. This is because the temperature on the hot side of the thermoelectric cooler becomes high. In those cases, an optimal heatsink, forced air/water cooling, or the like is required. Thermoelectric coolers are designed to cool a CCD efficiently when used at less than or equal to 60% of the maximum current.

As a rough guide, CCDs are cooled to the following temperatures when the ambient temperature is 25 °C.

· One-stage TE-cooled type: about 0 to -10 °C
· Two-stage TE-cooled type: about -20 to -30 °C
· Four-stage TE-cooled type: about -50 to -70 °C

To ensure stable and reliable operation, the thermoelectric cooler current and heat dissipation condition should be determined according to the surrounding environment.

[Figure 1-19] Cooling characteristics of one-stage thermoelectrically cooled type (S7171-0909-01)



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TDI-CCD

Back-thinned TDI (time delay integration)-CCDs allow acquiring high S/N images even under low-light conditions during high-speed imaging and the like. TDI operation yields dramatically enhanced sensitivity by integrating the exposure of a moving object. The back-thinned structure ensures high quantum efficiency over a wide spectral range from the ultraviolet to the near infrared region (200 to 1100 nm).

◉ TDI operation

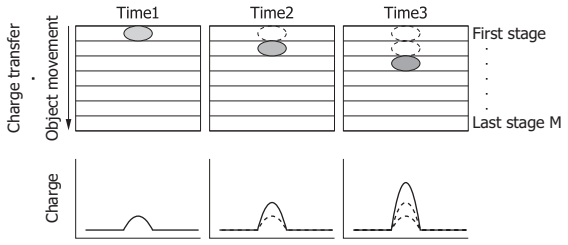
In CCD operation, a signal charge is transferred to the output section while being held in potential wells so as not to mix with other individual charges. TDI operation makes good use of this CCD charge transfer principle, and it is an effective technique for detecting weak light and for imaging a moving object or a still object while scanning it with a CCD sensor that is itself being moved.
Normally, an image focused on the CCD sensor is output as a signal corresponding to the focused position. This means that the image focused within the integration time must stay in the same position on the CCD sensor. If, for some reason, the focused position is shifted, then the image S/N will deteriorate. When an object is moving, the focused position will shift, causing the image to blur or, in some cases, no image to appear.
The TDI operation, in contrast, is a unique operation that captures images of a moving object. In FFT-CCD, signal charges in each column are vertically transferred during charge readout. TDI operation synchronizes this vertical transfer timing with the movement of the object, so signal charges are integrated by a number of times equal to the number of vertical stages of the CCD pixels.
In TDI operation, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by equation (2).

$$v = f \times d \cdots\cdots (2)$$

v: object speed, charge transfer speed
f : vertical CCD transfer frequency
d: pixel size (transfer direction)

In Figure 1-20, when the charge accumulated in the first stage is transferred to the second stage, another charge produced by photoelectric conversion is simultaneously accumulated in the second stage. Repeating this operation continuously until reaching the last stage M (number of vertical stages) results in a charge accumulation M times greater than the initial charge. This shows that the TDI operation enhances sensitivity up to M times higher than ordinary linear image sensors. (If the number of vertical stages is 128, the sensitivity will be 128 times higher than ordinary linear image sensors.) Since the accumulated signal charges are output for each column from the CCD horizontal shift register, a two-dimensional continuous image can be obtained. TDI operation also improves sensitivity variations compared to two-dimensional operation mode.

[Figure 1-20] Schematic of integrated exposure in TDI operation



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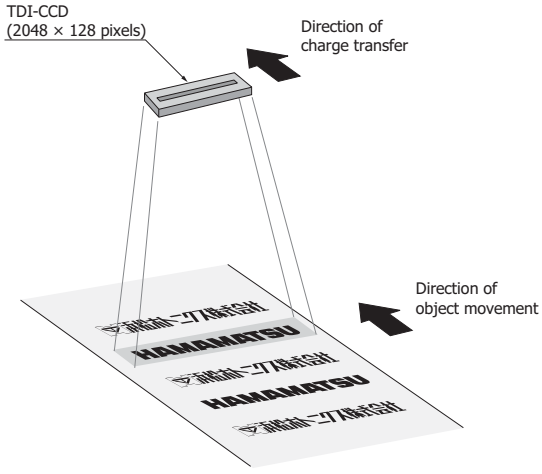
[Figure 1-21] Imaging examples in TDI operation

(a) Imaging of fast moving object



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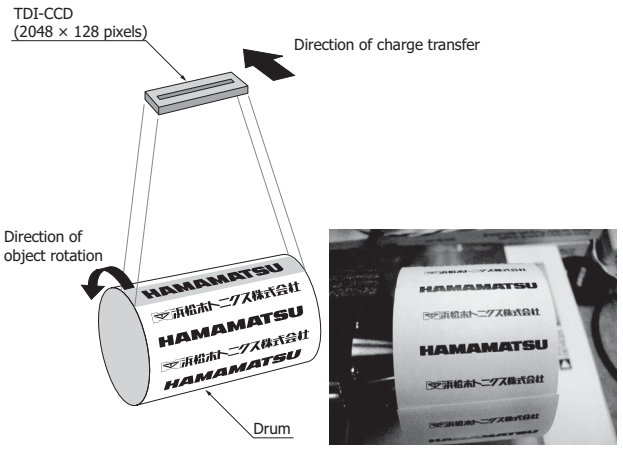
(b) Imaging of fast rotating object



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In Figure 1-21 (b), when the CCD is put in two-dimensional operation and the drum is imaged while in idle, a clear image with no blurring is obtained as shown in Figure 1-22 (a). However, when the drum is rotating, the image is blurred as shown in Figure 1-22 (b). Shortening the shutter time captures an unblurred image, but the image becomes dark as shown in Figure 1-22 (c). Using a TDI-CCD acquires clear, continuous images with no blurring as shown in Figure 1-23 since charge transfer is performed in the same direction at the same speed as those of the rotating drum.

[Figure 1-22] Imaging in two-dimensional operation

(a) When drum is in idle

(b) When drum is rotating

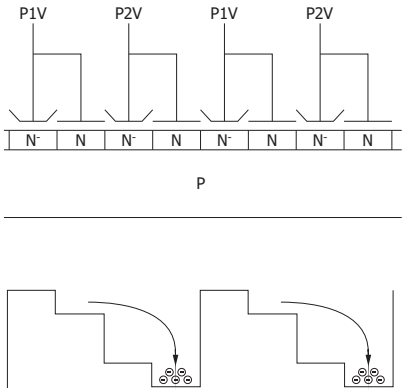
(c) When drum is rotating (with shutter time shortened)

[Figure 1-23] Imaging in TDI operation
(continuous image during drum rotation)

Resistive gate structure

In ordinary CCDs, one pixel contains multiple electrodes and a signal charge is transferred by applying different clock pulses to those electrodes [Figure 1-24]. In resistive gate structures, a single high-resistance electrode is formed in the photosensitive area, and a signal charge is transferred by means of a potential slope that is created by applying different voltages across the electrode [Figure 1-25]. Compared to a CCD area image sensor which is used as a linear sensor by line binning, a CCD linear image sensor having a resistive gate structure in the photosensitive area offers higher speed transfer, allowing readout that leaves behind fewer unread charges even if the pixel height is large.

[Figure 1-24] Schematic and potential of ordinary 2-phase CCD



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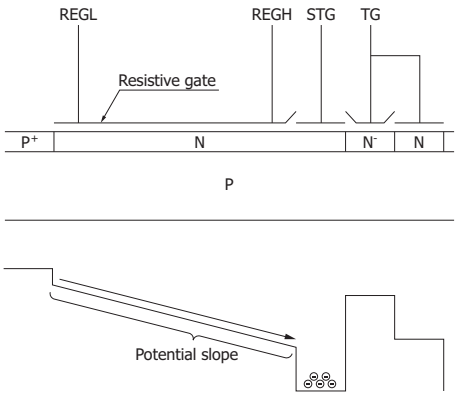
[Figure 1-25] Schematic and potential of resistive gate structure



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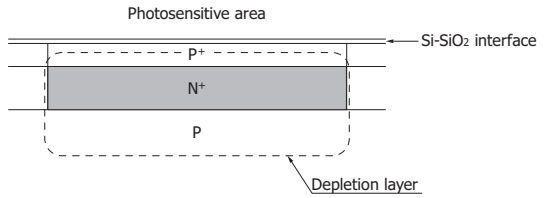
Buried photodiode

In the case of a CCD linear image sensor that uses a photodiode structure in the photosensitive area, low dark current can be achieved by buried photodiodes. The buried photodiode has a P^+N^+P structure with a thin P^+ diffusion layer formed on the surface of the photosensitive area [Figure 1-26]. Since the depletion layer is distant from the Si-SiO_2 interface, the dark current can be reduced to a level equivalent to that of a CCD in MPP operation.

[Figure 1-26] Cross section (buried photodiode)



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1 - 2 Characteristics

Conversion factor

The conversion factor is the charge-to-voltage conversion ratio of an FDA.
The FDA converts a signal charge into a voltage, which is output from the output end OS as the voltage ΔVout.

$$\Delta Vout = Av \times Q / Cfd \cdots\cdots (3)$$

Av : voltage gain of charge-to-voltage conversion MOSFET
Q : signal charge [C]
Cfd: node capacitance [F]

The conversion factor (Sv) is expressed by equation (4).

$$Sv = q \times \Delta Vout / Q \ [V/e^-] \cdots\cdots (4)$$

q: electron charge
When the S7030/S7031 series is used: Sv=2.2 μV/e⁻
When the S11071 series is used: Sv=8.0 μV/e⁻

The node capacitance (Cfd) is expressed by equation (5).

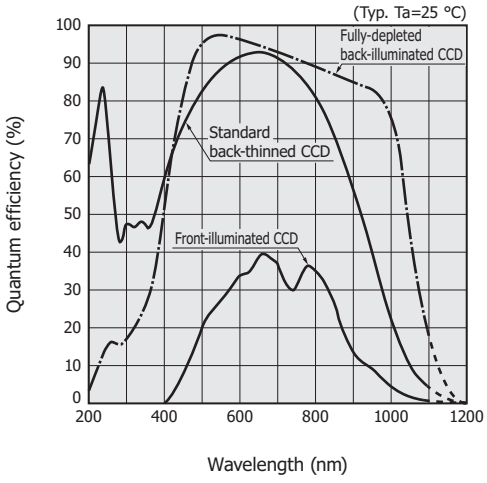
$$Cfd = q \times Av / Sv \ [F] \cdots\cdots (5)$$

When the S7030/S7031 series is used: Cfd=48 fF
When the S11071 series is used: Cfd=12 fF

Spectral response

Figure 1-27 shows the spectral response of front-illuminated CCDs and back-illuminated CCDs. Front-illuminated CCDs have no sensitivity in the ultraviolet region, and the maximum quantum efficiency in the visible region is approx. 40%. In contrast, standard back-thinned CCDs deliver very high quantum efficiency, which is 40% or higher in the ultraviolet region and approx. 90% at a peak wavelength in the visible region. The fully-depleted back-illuminated CCDs use a thick silicon substrate which allows higher sensitivity in the wavelength range from 800 to 1100 nm than standard back-thinned CCDs. The fully-depleted back-illuminated CCDs also have high sensitivity in the visible region from 400 to 700 nm due to use of a special AR (anti-reflection) coating process; however the ultraviolet sensitivity is low. The spectral response range is determined on long wavelengths by the silicon substrate thickness and on short wavelengths by the sensor structure on the light input surface side. Front-illuminated FFT-CCDs require that poly-silicon gate electrodes be formed on the effective photosensitive area because of their structure, which makes the CCD almost insensitive to ultraviolet light at wavelengths shorter than 400 nm. To make it sensitive to ultraviolet light, a scintillator material called "Lumogen" is coated on the CCD surface of some front-illuminated types. Back-illuminated CCDs, on the other hand, deliver a high quantum efficiency from ultraviolet region to near infrared region and also exhibit excellent stability even during exposure to ultraviolet light.
In the near infrared region at wavelengths longer than 700 nm, the quantum efficiency of standard front-illuminated CCDs is not so high (this depends on the depletion layer thickness), but the near infrared enhanced front-illuminated CCD delivers high quantum efficiency even in the near infrared region [Figure 1-28].
When a CCD is cooled during use, it should be noted that the sensitivity drops at wavelengths longer than approx. 800 nm [Figure 1-29].

[Figure 1-27] Spectral response (without window)



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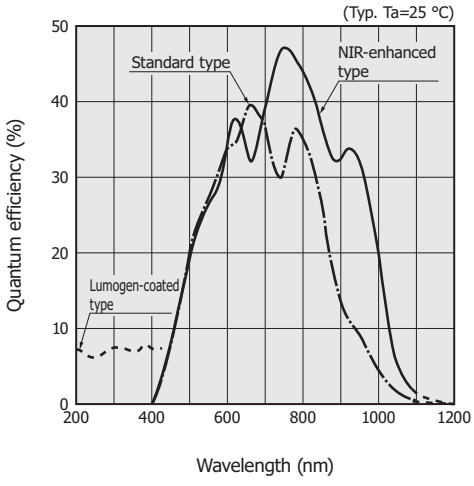
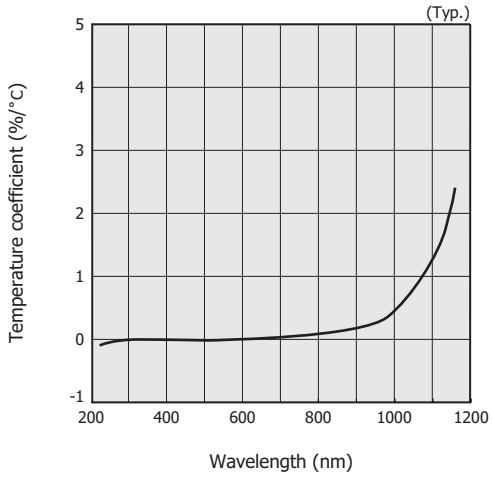
[Figure 1-28] Spectral response of front-illuminated CCDs (without window)



KMPDB0205EC

[Figure 1-29] Temperature characteristics of sensitivity (S7031 series)



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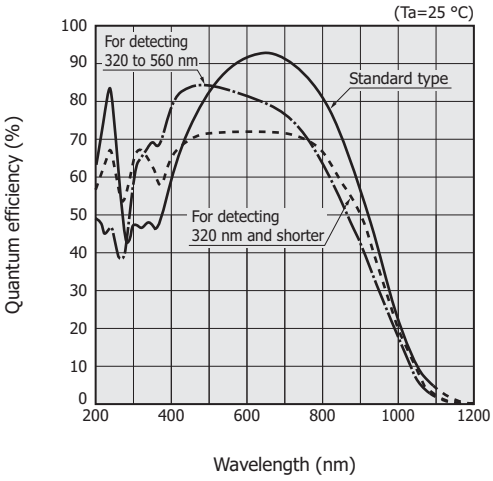
(1) Back-thinned CCD with optimized spectral response

With the back-thinned CCD, various spectral responses can be achieved by optimizing the anti-reflection film on the photosensitive surface [Figure 1-30].

[Figure 1-30] Spectral response (back-thinned CCDs, without window, typical example)



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(2) Front-illuminated CCD linear image sensor with stable spectral response in the ultraviolet region

The spectral response in the ultraviolet region of front-illuminated CCDs that are designed to be sensitive in the ultraviolet region had been inconsistent depending on the element. We have developed the S11151-2048 front-illuminated CCD linear image sensor that suppresses inconsistencies between different elements in the spectral response in the ultraviolet region by fabricating a special structure in the photosensitive area.

(3) Lumogen-coated front-illuminated CCD

The photosensitive area of front-illuminated CCDs is covered with poly-silicon electrodes. Ultraviolet light is almost totally absorbed by the poly-silicon, so the quantum efficiency in the ultraviolet region is nearly zero. To make the front-illuminated CCDs sensitive to ultraviolet light, a scintillator material “Lumogen” is sometimes used for coating. Lumogen is directly coated on the CCD effective photosensitive area by vacuum sublimation.

Lumogen absorbs light at wavelengths shorter than 480 nm and emits light whose center wavelength is around 530 nm. In other words, ultraviolet light striking the CCD surface is converted to visible light by the Lumogen scintillator, and this light is then detected by the CCD.

Care should be taken when using a Lumogen-coated front-illuminated CCD because its life under ultraviolet light is extremely short and its sensitivity is highly dependent on temperature when compared to back-thinned CCDs.

Selecting window materials

Back-thinned CCDs provide high quantum efficiency over 90% at the peak sensitivity wavelength around 700 nm, but this is a value measured without a window.

The quantum efficiency of CCDs is affected by the window material. Hamamatsu mainly uses three types of windows for CCDs: AR (anti-reflection) coated sapphire (S type), quartz (Q type), and windowless (N type).

Sapphire is mechanically strong and scratch-resistant compared to quartz and is stable in high humidity environments. In addition, since the thermal conductivity of sapphire is close to that of metal, it is less likely to cause moisture condensation and can be hermetically sealed within a metal package, making it an excellent choice as window material. The transmittance of sapphire having no AR coating is not so high, but AR coated sapphire has good transmittance which is higher than quartz in the visible region. Hamamatsu thermoelectrically cooled CCDs such as the S9971/S7031 series use sapphire as a standard window material.

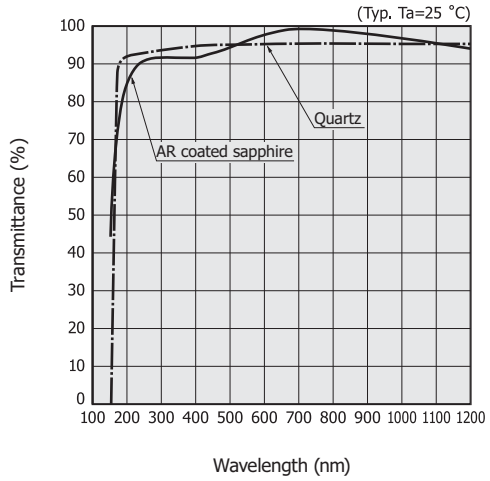
Quartz is available in two types: synthetic quartz and fused quartz. Synthetic quartz is more frequently used as the window for CCDs since it contains fewer metallic impurities. Even if there is no AR coating, quartz has high transmittance which is approx. 94% in the visible region. Quartz transmits light down to a wavelength of 200 nm or shorter and so is suitable as a window material, especially when detecting ultraviolet light. However, in the past when quartz was used as a window of a cooled CCD, consideration had to be given to condensation that may form within the package due to the moisture permeability of the adhesive resin. Using new technology, we have made it possible to hermetically seal the package without using adhesive resin for the quartz window.

Naturally, CCDs not having a window exhibit the highest quantum efficiency. Windowless CCDs are sometimes used especially in the vacuum ultraviolet region at wavelengths shorter than 160 nm because appropriate window materials are not available in that region.

Other window materials include borosilicate glass which is less expensive than quartz. Borosilicate glass is mainly used to detect visible and longer wavelength light since its transmittance sharply drops from wavelengths around 300 nm. To detect X-rays, aluminum or beryllium

is used as the window material which allows X-rays to transmit through but blocks out light (use caution since beryllium is toxic).

[Figure 1-31] Spectral transmittance of window materials



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Photoresponse nonuniformity

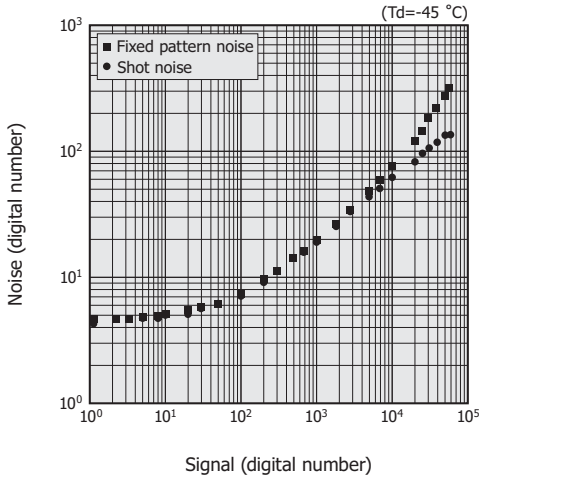
Photoresponse nonuniformity specifies the variations in sensitivity between pixels of a CCD, and is caused by variations in the light input window and the wafer process. Noise accompanying the photoresponse nonuniformity is proportional to the signal level.

A photon transfer curve [Figure 1-32], which plots the relationship between the noise and the input signal level varying with light exposure, is acquired by illuminating the effective photosensitive area with uniform light and setting a measurement area of about 50 × 50 pixels. Photoresponse nonuniformity (PRNU) is then defined by equation (6).

$$PRNU = \frac{Noise}{Signal} \times 100\ [\%] \cdots\cdots\cdots (6)$$

Here, noise is a statistical value indicating the standard deviation of pixel signals. The signal is the average signal of each pixel in the effective photosensitive area. When the signal level is low, the PRNU is affected by shot noise (see “Noise” in section 1-2, “Characteristics”). However, when the signal level is sufficiently high, the PRNU becomes a constant value. The PRNU specified in our datasheets was measured at a signal level that is 50% of the saturation charge. A PRNU of typical FFT-CCDs is approx. 1% rms or ±3% typ. (peak to peak).

[Figure 1-32] Photon transfer curve (S9974-1007, typical example)



KMPDB0210EA

Saturation charge

The saturation charge for a CCD indicates the number of signal electrons that can be transferred by a potential well. This saturation charge is expressed in units of e^-.

The saturation charge for CCDs is determined by the following four factors:

- Vertical shift register saturation charge (vertical full well capacity)
- Horizontal shift register saturation charge (horizontal full well capacity)
- Summing saturation charge
- Output section saturation charge

In two-dimensional operation mode, the signal charge of each pixel is output individually, so the saturation charge is determined by the vertical shift register. On the other hand, the horizontal saturation charge is designed to saturate at a higher level than the vertical saturation charge so as to enable line binning. The summing saturation charge formed by the summing gate, which is the last clock gate, is designed to be greater than the horizontal saturation charge in order to add signals from the horizontal shift register (pixel binning).

The saturation voltage (Vsat) of an output signal is given by equation (7).

$$Vsat = FW \times Sv \cdots\cdots\cdots (7)$$

FW: full well capacity (saturation charge)
Sv : conversion coefficient

Linearity

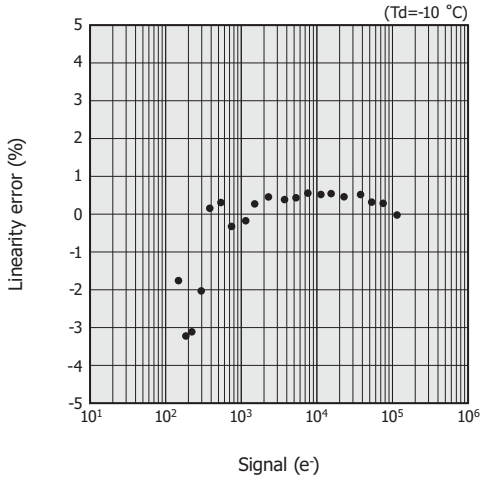
Linearity of CCD output characteristics deviates slightly from the ideal line γ=1. The cause of this deviation is related to the output stage and results from capacitive variations in the reverse-biased PN junction constituting the FDA and from fluctuations of the MOSFET transconductance.

The extent of linearity deviation is expressed in terms of linearity residual (LR) as defined by equation (8).

$$LR = \left(1 - \frac{Sm/Tm}{S/T}\right) \times 100\ [\%] \cdots\cdots (8)$$

Sm: signal level at one-half the saturation charge
Tm: exposure time at one-half the saturation charge
S : signal
T : exposure time

[Figure 1-33] Linearity (S9971-1007, two-dimensional operation mode, typical example)



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Charge transfer efficiency

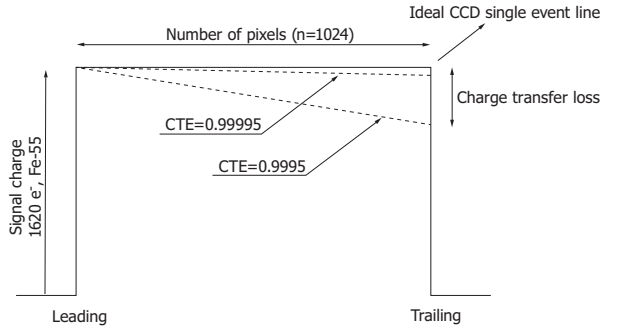
Ideally, there is no loss in the charge transfer process of CCDs. In actual operation, however, 100% charge transfer is not attained due to traps resulting from the semiconductor materials and wafer process. A very small amount of charge is not transferred and is left behind.
Charge transfer efficiency (CTE) is defined as the ratio of charge that is transferred from one pixel to the adjacent pixel. (In a 2-phase CCD, 2 charge transfers are required in gate units in order to transfer the signal charge per pixel, but those two transfers are specified as one transfer.)
An X-ray stimulation method is effective in measuring the transfer efficiency of a small charge because X-ray incident on the CCD causes an ideal spot charge to be input in a pixel without using electrical means.
In this measurement, the signal of each line in the horizontal direction is stacked (horizontal stacking). By means of this horizontal stacking, the CCD output depicts a single event line according to the X-ray energy as shown in Figure 1-34. In an ideal CCD with a CTE equal to 1, the signal height of the leading and trailing edges would be the same. In actual use, however, the CTE is less than 1, so a loss of the signal charge transfer occurs at the trailing edge. If we let the signal charge at the leading edge be 1, then the charge transfer loss is expressed by equation (9).

$$\text{Charge transfer loss} = n \times CTI \cdots\cdots (9)$$

n: number of pixels
CTI (charge transfer inefficiency) = 1 - CTE

The CTE of standard Hamamatsu CCDs is 0.99999.

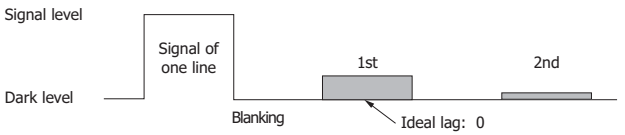
[Figure 1-34] CTE evaluation method by Fe-55 stacking



KMPDC0046EA

Interline CCDs experience image lag in the order of several percent due to the incomplete transferring of signals from the photodiodes to the shift register. On the other hand, in the case of an FFT CCD in which the shift register itself receives light, image lag is generated due to the trapping and discharging of signal charges by the traps (see "Damage by radiation" in section 1-3, "How to use"). As a result, this image lag is observed as a CTE deterioration. Here CTE image lag is described briefly using line binning as an example.
In line binning, signals are acquired for each line corresponding to the number of horizontal shift registers. If the CTE is 1 (the ideal case), the signal charge in the readout after a line signal is equal to the dark level. But, if the CTE is less than 1, unread signal charges will be left behind as shown in Table 1-1 depending on the number of transfers.

[Figure 1-35] CCD image lag in line binning



KMPDC0047EB

[Table 1-1] Charge transfer efficiency and ratio of image lag in line binning

CTE	S9971-0906	S9971-0907
0.99995	0.0032	0.0064
0.99999	0.00064	0.00128
0.999995	0.00032	0.00064

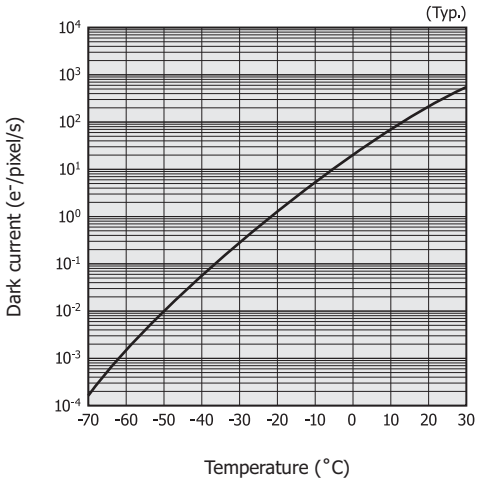
Dark current

Dark current is an output current that flows when no light is input. This is generally expressed in units of A (ampere), A/cm², and V (volt). In CCDs for measurement applications, e⁻/pixel/s or e⁻/pixel/h units are generally used, which indicate the number of electrons generated in one pixel per unit time. Dark current nearly doubles for every 5 to 7 °C increase in temperature.
Three major causes that generate CCD dark current are as follows:

① Thermal excitation and diffusion in undepleted region
② Thermal excitation in depletion layer
③ Thermal excitation by surface level

Among these three causes, item ③ is most dominant.
MPP (multi-pinned phase) operation reduces the dark current and is also referred to as inverted operation. MPP operation is performed by setting the portions under all MOS structure gates, which constitute the CCD electrodes, to the inverted state.
The dark current can be significantly lowered by MPP operation since it suppresses the effect of ③ .

[Figure 1-36] Dark current vs. temperature (S9970/S9971 series)



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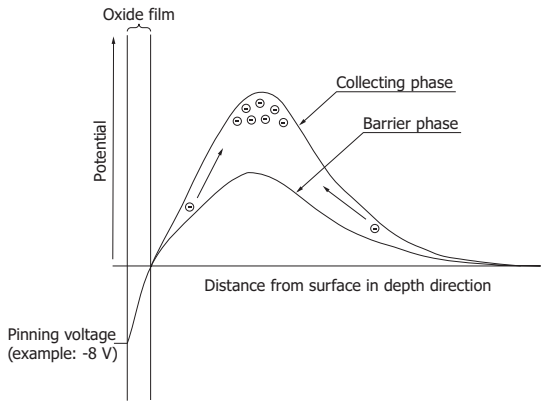
In a 2-phase CCD, a potential difference is applied between the barrier phase and the signal charge collecting phase by way of ion implantation and the like. The 2-phase CCD therefore provides the potential wells for accumulating charges even when all gates are set to the same voltage. MPP operation can be performed by applying a bias to invert all phases of the CCD.
When the dark current must be reduced, using the MPP operation and cooling the CCD are very effective.

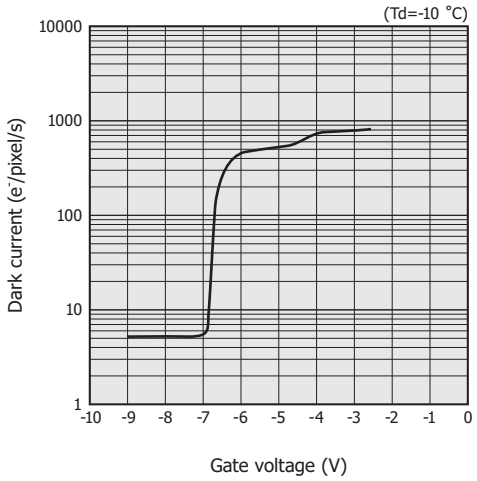
[Figure 1-37] Potential distribution in MPP operation



KMPDB0055EB

As shown in Figure 1-37, during MPP operation, both the collecting phase and barrier phase are pinned in the inverted state. In the pinned state, the CCD surface is inverted by holes supplied from the channel stop region. The potential at the oxide film interface is fixed at the same potential as the substrate, even if a further negative voltage is applied.
In the state where the oxide film interface is inverted by holes, the generation of thermally excited electrons is drastically suppressed. This therefore allows attaining a state with low dark current.

[Figure 1-38] Dark current vs. gate voltage (S9974-1007, typical example)



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In MPP operation, the dark current can be greatly reduced by applying the optimum pinning voltage. However, if the voltage does not reach the optimum pinning voltage, the inverted layer is not fully formed by holes, so the dark current cannot be minimized. In contrast, if the voltage is increased as a negative value in excess of the optimum pinning voltage, not only is extra clock amplitude required, but the dark current may also increase due to excessive charges called spurious charges (see “Spurious charges” in section 1-2, “Characteristics”). Dark current can be minimized by adjusting the voltage to an optimum value near the gate voltage listed in the datasheet.

Noise

CCD noise is classified into the following four factors:

(1) Fixed pattern noise (Nf)

This noise is caused by variations in sensitivity between CCD pixels (variations in sensitivity between pixels is caused by nonuniformities in the aperture area and film thickness). When the signal is large, the fixed pattern noise is proportional to the amount of exposure (number of signal electrons). The fixed pattern noise Nf can be regarded as zero based on the noise from one pixel.

(2) Shot noise (Ns)

Shot noise is the noise generated by statistical changes in the number of photons incident on a CCD. Shot noise is expressed by equation (10) according to the Poisson distribution.

$$Ns = \sqrt{S} \cdots\cdots (10)$$

S: number of signal electrons [e⁻]

For example, if a CCD receives photons that generate a signal electron quantity of 10000 e^- inside the CCD, then the shot noise will be 100 e^- rms.

(3) Dark shot noise (Nd)

Dark shot noise is caused by dark current and is proportional to the square root of the number of electrons generated in a dark state. To reduce the dark shot noise, the dark current itself must be reduced. The variation in dark current between each pixel is larger than variations in the sensitivity.

(4) Readout noise (Nr)

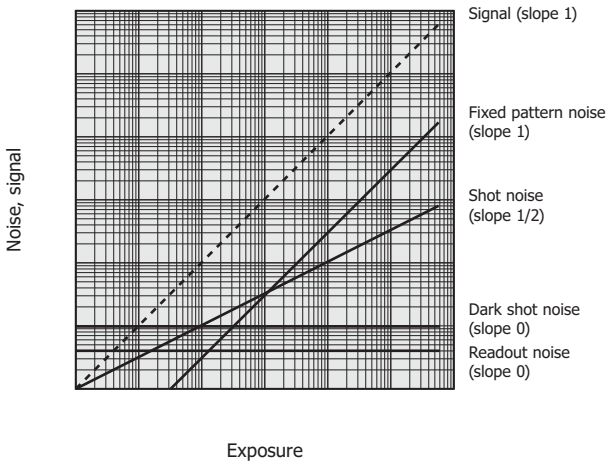
This is electrical noise from thermal noise caused by the MOSFET used as the amplifier in the CCD output section. It also comes from the readout circuit and eventually determines the lower detection limit of the CCD. Readout noise is determined by the CCD output method and is not affected by the amount of exposure. Readout noise is also frequency dependent [Figure 1-43].

Total noise (Nt) is expressed by equation (11).

$$Nt = \sqrt{Nf^2 + Ns^2 + Nd^2 + Nr^2} \cdots\cdots\cdots (11)$$

Figure 1-39 shows the interrelation between these four factors and the amount of exposure. The CCD detection limit is determined by the dark shot noise and readout noise. This means that the CCD detection limit can be lowered to the readout noise level by reducing the dark current and lowering the dark shot noise below the readout noise.
The S/N is mainly determined by the fixed pattern noise when the amount of exposure is high, and it is determined by the shot noise when the amount of exposure is low.

[Figure 1-39] Noise vs. exposure



Dynamic range

Dynamic range generally specifies the measurable range of a detector and is defined as the ratio of the maximum level to the minimum level (detection limits).

The CCD dynamic range is a value obtained by dividing the saturation charge by the readout noise.

$$\text{Dynamic range} = \frac{\text{Saturation charge}}{\text{Readout noise}} \cdots\cdots\cdots (12)$$

Dynamic range is also given by equation (13).

$$\text{Dynamic range} = 20 \times \log\left(\frac{\text{Saturation charge}}{\text{Readout noise}}\right) \text{[dB]} \cdots (13)$$

The dynamic range varies with operating conditions such as operating temperature and integration time. At around room temperature, the dark shot noise determines the lower detection limit. Under operating conditions where the dark shot noise can be ignored (by cooling the CCD sufficiently), the readout noise determines the dynamic range.
In two-dimensional operation, the saturation charge will equal the charge that can be transferred by the vertical shift register. In line binning, the saturation charge will equal the charge that can be transferred by the horizontal shift register.

[Table 1-2] CCD specification examples

Parameter	S9736 series	S7170-0909
Type	Front-illuminated type	Back-thinned type
Number of pixels	512 × 512	
Pixel size [μm]	24	
Saturation charge (vertical) [ke⁻]	300	320
Conversion factor [μV/e⁻]	3.5	2.2
Readout noise [e⁻ rms]	4	8
Dynamic range	75000	40000
Dark current (0 °C) [e⁻/pixel/s]	10	

Resolution

The ability of an image sensor to reproduce the contrast at a spatial frequency in an image is called the spatial resolution and is quantified by the MTF (modulation transfer function) for sine waves. Since the pixels of a CCD are individually separated, there is a limiting resolution determined by the Nyquist limit due to the discrete sampling theorem. For example, when a black-and-white stripe pattern is viewed with a CCD, the difference between the black and white signal levels decreases as the stripe pattern becomes finer, and finally reaches a point at which the stripe pattern cannot be resolved. The ideal MTF of CCDs is expressed by equation (14).

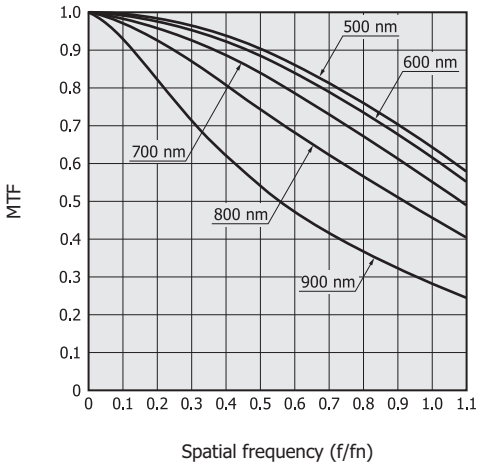
$$MTF = \text{sinc}\{(\pi \times f)/(2 \times fn)\} \cdots\cdots\cdots (14)$$

f : spatial frequency of image
fn: spatial Nyquist frequency

Because optical sine waves are difficult to generate, a test chart having square wave patterns is commonly used. The spatial frequency response measured using this test chart is called the contrast transfer function (CTF) which

is different from the MTF. (The CTF can be converted into the MTF by Fourier transform.)
The actual CCD resolution is determined by the extent of diffusion occurring when the signal charge is collected inside the silicon. Since the incident photons are absorbed within the depletion layer, the generated electrons do not diffuse and is collected by the corresponding pixels, so the resolution does not deteriorate. The resolution also varies depending on the depth in the silicon where the incident photons are absorbed. The longer the incident photon wavelength, the deeper the position where the photons are absorbed, causing the resolution to deteriorate.

[Figure 1-40] MTF vs. spatial frequency at different wavelengths of input photons (S9970/S9971 series, calculated values)



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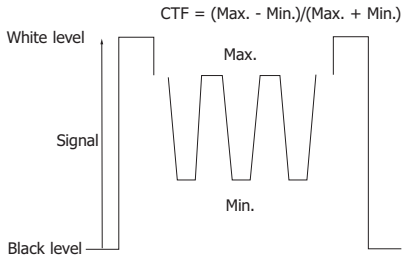
[Figure 1-41] CTF calculation method



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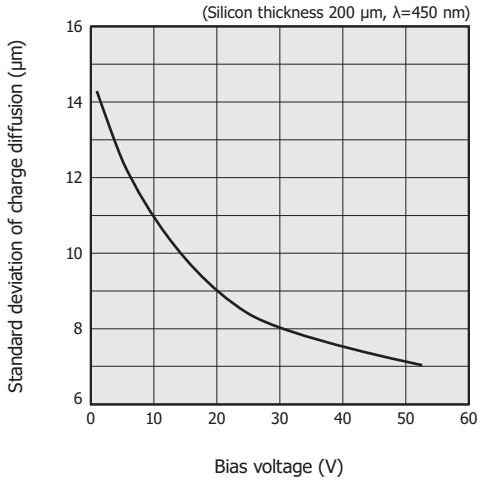
Point spread function

The standard deviation (σ_D) of charge diffusion in the depletion layer is defined as shown in equation (15). Here, σ_D is proportional to the square root of the depletion layer thickness and also of the absolute temperature in the silicon, and is inversely proportional to the square root of the bias voltage applied to the backside.

$$\sigma_D = \sqrt{\frac{2 \times Xdep^2 \times k\ T}{Vbb \times q}} \quad \cdots\cdots\cdots (15)$$

Xdep: thickness of depletion layer
k : Boltzmann's constant
T : absolute temperature
Vbb : bias voltage applied to backside
q : electron charge

[Figure 1-42] Standard deviation of charge diffusion vs. bias voltage

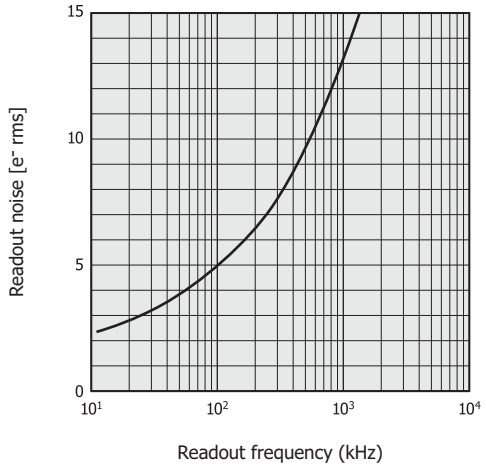


KMPDB0281EB

Frequency characteristics of noise

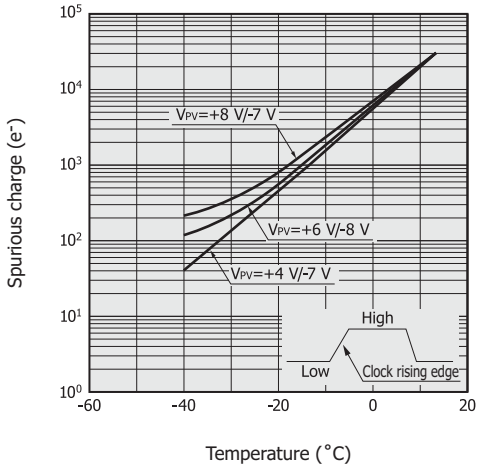
When dark current and spurious charges are sufficiently small, the readout noise determines the eventual number of noise electrons generated in a CCD. The readout noise is determined by the thermal noise of the MOSFET comprising the FDA in the readout section. MOSFET thermal noise includes white noise and 1/f noise, both of which should be reduced to achieve low noise. White noise can be reduced by increasing the MOSFET mutual conductance (gm). In MOSFET built into CCDs for measurement applications, the corner frequency of 1/f noise is reduced to as low as a few kilohertz.
MOSFET thermal noise depends greatly on the bias conditions. To achieve the readout noise specified in our CCD image sensor datasheet, the bias must be applied according to the recommended operating conditions. Even when the recommended bias conditions have been set, the signal processing circuit still has a great effect on CCD readout noise. Since a CDS circuit is commonly used for CCD signal processing, optimizing the transfer functions for the CDS circuit and the LPF (low-pass filter) installed in the preceding stage of the CDS circuit will result in reduced CCD readout noise. If the effect of the 1/f noise corner frequency can be reduced versus CCD readout frequency, then the output noise of the CCD system including the signal processing circuit will be determined by the white noise and noise bandwidth.
To summarize the above, CCD readout noise depends on the readout frequency. The readout frequency must be low (less than 100 kHz) to achieve a readout noise of a few electrons (e^- rms) which is a noise level required in measurement applications. If the signal readout frequency becomes higher, the readout noise increases sharply.

[Figure 1-43] Readout noise vs. readout frequency (S9737-01, typical example)



KMPDB0207EA

[Figure 1-44] Spurious charge vs. temperature (typical example)



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Spurious charge

Spurious charges are generated by clock pulses during operation such as in MPP mode and do not result from signals produced by the incident light. In MPP operation, the vertical clock pulse is set to low, and during this low period, the region under the gate of each pixel is in an inverted state. In this state, holes move from the channel stop region to a point under the gate, and the surface potential in that region is pinned at the substrate potential. At this point, some holes are trapped along the oxide film interface, and the gate phase of each pixel becomes a non-inverted state when the clock pulse goes to high level. The trapped holes have high energy after being released and generate a spurious charge which is then collected in a potential well. The CCD output is the sum of the signal, dark current, and this spurious charge. Spurious charges can be reduced by delaying the rising edge of clock pulses or decreasing the voltage difference between high and low clock levels. When a CCD is cooled to a sufficiently low temperature where the signal level approaches readout noise level, it is important to set the clocking conditions by taking the spurious charge into account.

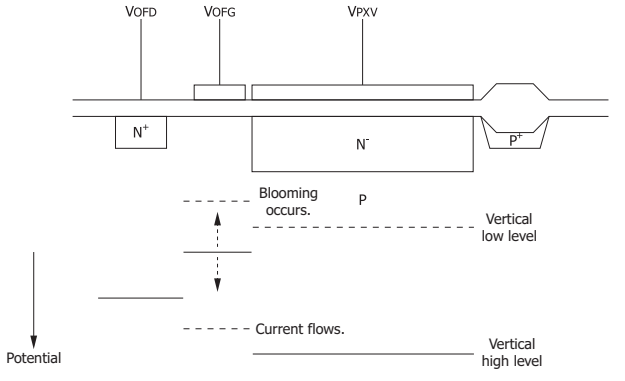
Anti-blooming

Blooming (overflow) is a phenomenon that occurs when high-intensity light enters the photosensitive area and the resulting signal charge exceeds a specific level. This excess charge then overflows into adjacent pixels and transfer region. A technique to prevent this is called anti-blooming which provides a drain to carry away the excess charge.

Anti-blooming structures for CCDs are roughly divided into a lateral type and a vertical type, and our CCDs use the lateral type. The lateral type structure has an overflow drain formed along the pixels or charge transfer channels. This structure has the drawback that the fill factor is reduced when used for front-illuminated CCDs. However, this problem can be avoided when used for back-thinned CCDs. The vertical type structure is designed so as to carry away the excess charge into the inside of the substrate. The fill factor is not reduced, but there is a problem in that the sensitivity drops at longer wavelengths.

When controlling the anti-blooming function by means of the overflow drain voltage (VOFD) and overflow gate voltage (VOFG), these applied voltages may decrease the saturation charge.

[Figure 1-45] Schematic of anti-blooming



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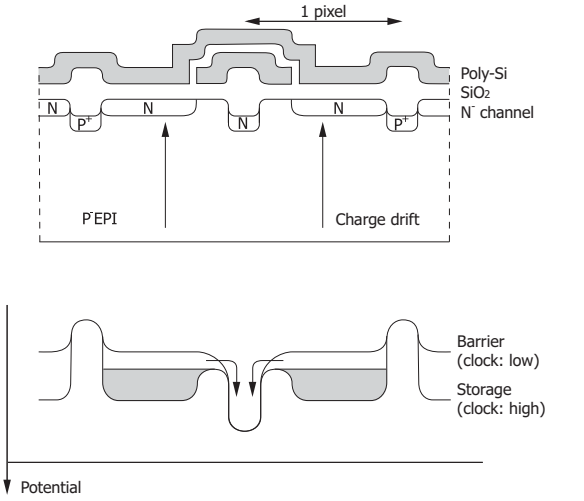
[Figure 1-46] Anti-blooming structure and potential (lateral type)



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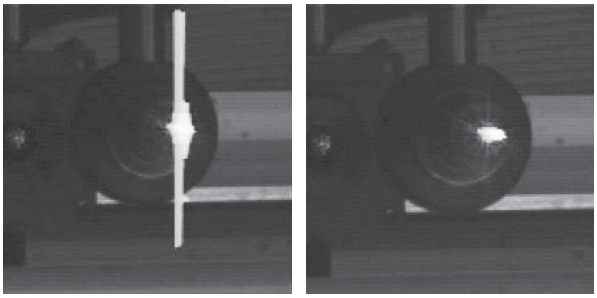
[Figure 1-47] Imaging examples

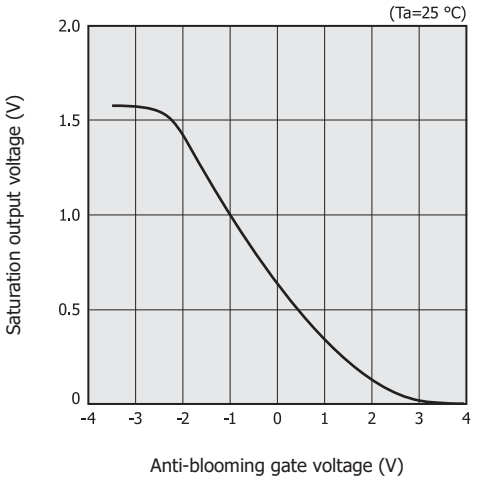
(a) Without anti-blooming (b) With anti-blooming



◉ Anti-blooming function of CCD linear image sensors

In CCD linear image sensors, an anti-blooming drain and anti-blooming gate are formed in the vicinity of the storage gate. The anti-blooming function works by applying appropriate voltage to the anti-blooming drain and anti-blooming gate. The anti-blooming gate voltage controls the saturation output voltage. Moreover, when the anti-blooming gate voltage is set high, all signal charges generated in the photodiodes can be extracted into the anti-blooming drain to make the output zero. This function is used to activate the electronic shutter described next.

[Figure 1-48] Saturation output voltage vs. anti-blooming gate voltage (typical example)



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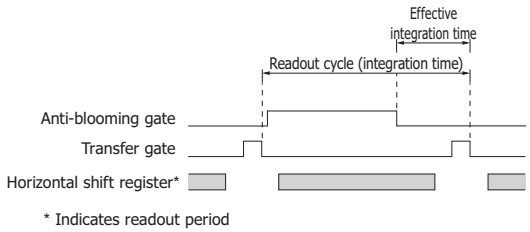
Electronic shutter

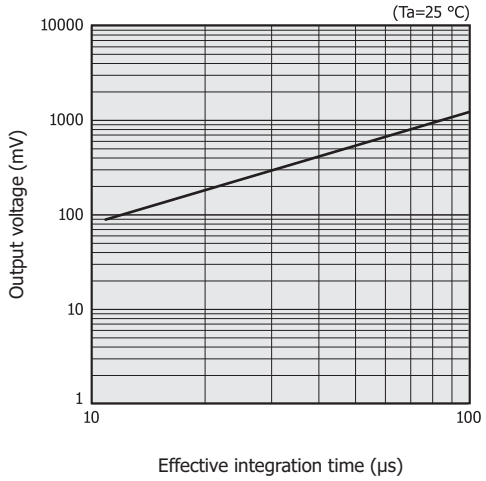
In general, the integration time for CCD linear image sensors is equivalent to the interval between two clock pulses to the transfer gate. Using an electronic shutter function allows setting an effective integration time that is shorter than the transfer gate clock pulse interval. When the anti-blooming gate voltage is set high, all signal charges generated in the photodiodes are carried away into the anti-blooming drain. It is therefore possible to set an effective integration time shorter than the normal integration time by providing a period during which the anti-blooming gate voltage is high and a period during which the anti-blooming gate voltage is low. In addition, the start timing of the integration time can be synchronized to an external trigger pulse.

[Figure 1-49] Timing chart for the CCD linear image sensor (electronic shutter function)



KMPDC0287EA

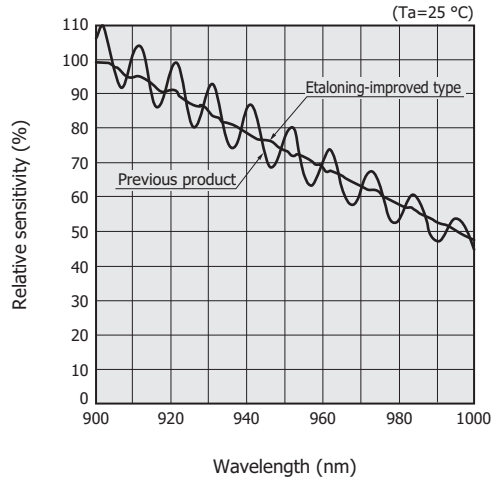
[Figure 1-50] Output voltage vs. effective integration time (CCD linear image sensor, typical example)



Etaloning

Etaloning is an interference phenomenon that occurs while the light incident on a CCD repeatedly undergoes reflection and attenuation between the front and back surfaces of the CCD, and causes alternately high and low sensitivity. An etalon commonly refers to an optical element consisting of two parallel planes with highly reflective films facing each other. The light entering a CCD repeatedly undergoes imperfect reflection, transmission, and absorption within the CCD as if the light has entered an etalon. This phenomenon is therefore called "etaloning." When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length [Figure 1-51]. Using our advanced device technology, we have succeeded in producing back-thinned CCDs that offer reduced etaloning. Note that etaloning is a phenomenon unique to back-thinned CCDs and does not occur in front-illuminated CCDs.

[Figure 1-51] Etaloning characteristics (typical example)



Cosmetics

The term "cosmetics" refers to the extent of CCD defects (blemishes and scratches). Blemishes and scratches are divided into two categories: "white spots" that appear bright in a dark state and "black spots" that appear dark when light is incident on a CCD.
White spots are usually caused by lattice defects or metal impurities in the substrate material or by pattern failures from mechanical damage or dust during the wafer process. Black spots are mainly caused by irregular reflections due to dust on the CCD surface during the wafer process or partial defects of the surface insulation film, or by contamination such as dust on the device surface or window. It is difficult to completely eliminate these white and black spots. The larger the photosensitive area and the smaller the pixel, the more obvious the effects from these white and black spots become.
Hamamatsu defines white and black spot specifications and inspects every CCD to check the number of these spots.
Cosmetic specifications are defined as described below. These definitions may vary depending on the manufacturer, so use caution when comparing specifications.

(1) Point defect

- White spot

White spots are pixels that generate dark current in excess of 3% of the saturation charge after charge integration for 1 second at a cooling temperature of 0 °C.

- Black spot

Black spots are pixels that provide an output of less than 50% of the average output value calculated when the CCD is illuminated with uniform light so as to generate a charge equal to 50 to 90% of the saturation charge. We usually perform this test using uniform light that generates a charge equal to 50% of the saturation charge.

(2) Cluster defect

A cluster consisting of two to nine continuous pixel defects is called a cluster defect and is distinguished from point defects. Cluster defects appear vertically in most cases, but appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS (fiber optic plate with scintillator).

(3) Column defect

A cluster consisting of ten or more continuous pixel defects (larger than a cluster defect) is called a column defect and is viewed as different from cluster defects. As with cluster defects, column defects also appear vertically in most cases, but may appear as a two-dimensional cluster if originating from black spots of back-thinned CCDs or front-illuminated CCDs coupled to an FOS.

Front-illuminated CCDs with a small photosensitive area, such as Hamamatsu S9970/S9971 series, have no point defects, cluster defects, or column defects. When CCDs are coupled to an FOP (fiber optic plate) or FOS, defects might occur due to other factors not originating in the CCDs, so the shape and number of defects will differ from those occurring only in CCDs.

Effects of cosmic rays on CCDs

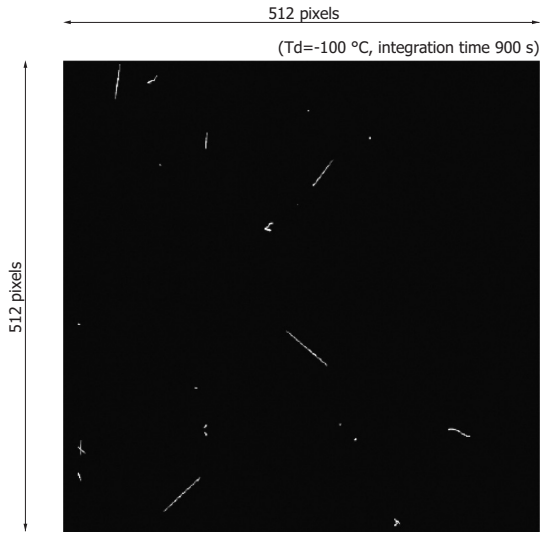
If cosmic rays enter the CCD, these rays may be detected as shown in Figure 1-52. A certain ratio of cosmic rays reaches the Earth's surface. The main portion of such rays consists of μ particles (up to several GeVs), and they generate signal charges inside the CCD silicon along their tracks. With the standard type back-thinned CCD, the silicon is thin, and therefore false signals due to cosmic rays will appear in only several pixels at most, but with the fully-depleted back-illuminated CCD, false signals may appear in many pixels.

The frequency at which cosmic rays are detected depends on the sensor structure or environment, but a rough estimate is 150 counts/(cm^2·h). It is known that the amount of cosmic rays increases as you move further away from the Earth's surface.

If false signals occur temporarily due to cosmic rays, their effects can be reduced by acquiring multiple images and averaging them or by reducing the integration time.

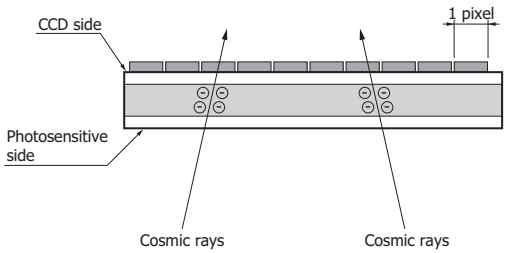
By interacting with silicon atoms, cosmic rays may cause lattice defects, and this phenomenon leads to white spots and charge traps. It is recommended that a correction function be provided in the device at the outset to deal with white spots.

[Figure 1-52] Image example of false signals caused by cosmic rays on fully-depleted back-illuminated CCD



[Figure 1-53] Cross section of CCD (back-illuminated) that has received cosmic rays

(a) Standard type



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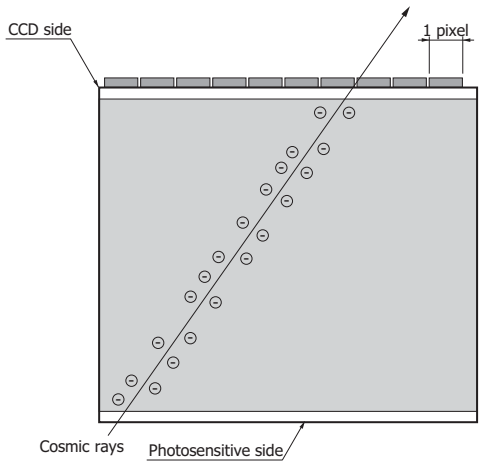
(b) Fully-depleted type



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1 - 3 How to use

Timing

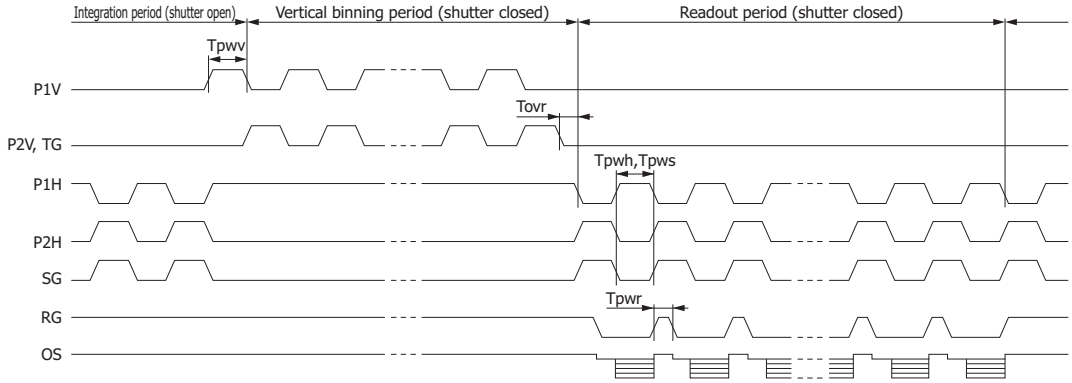
Operating a CCD requires seven types of signals: 2-phase clock pulses (P1V, P2V) for the vertical shift register, a transfer gate pulse (TG), 2-phase clock pulses (P1H, P2H) for the horizontal shift register, a summing gate pulse (SG), and a reset pulse (RG). The TG electrode utilizes a part of the last P2V electrode but is recommended to be used as a separate terminal where the clock pulse should be input at the same timing as P2V. However, operation is also possible by shorting the TG and P2V terminals. To find timing charts of pulses needed to operate a CCD, refer to our datasheet.

FFT-CCDs can be operated in any of four modes: line binning, two-dimensional operation, pixel binning, or TDI operation. The desired operation mode can be chosen by simply adjusting the timing of each clock pulse.

(1) Line binning

The number of bits that should be “binned” is first transferred in the vertical direction. This permits signal charges to be added to the corresponding horizontal shift register. Then all horizontal signal charges are transferred. The summing gate pulse should be exactly the same as the clock pulse (P2H) for the horizontal shift register.

[Figure 1-54] Timing chart of line binning



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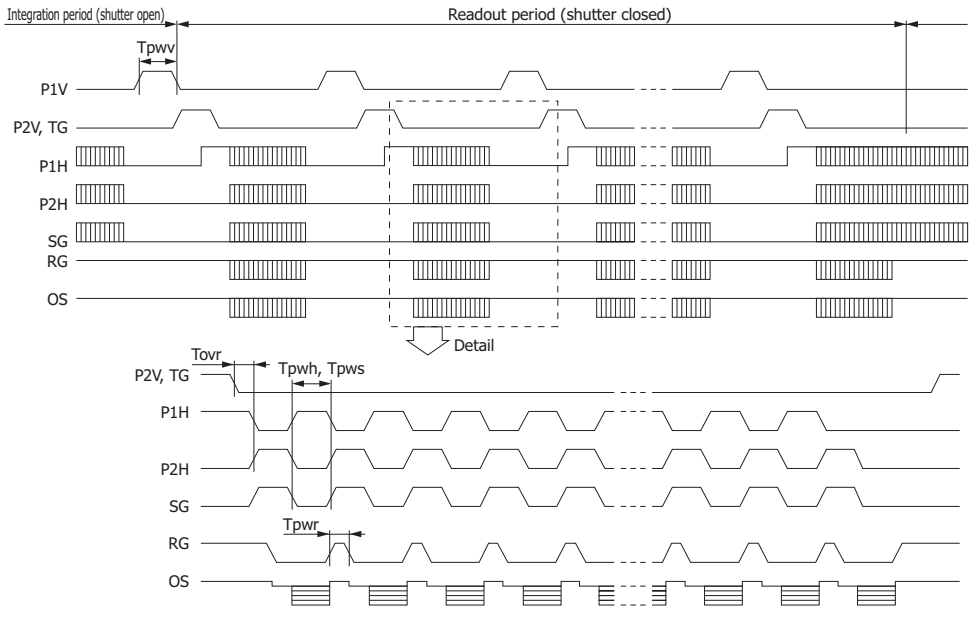
Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*1	Pulse width	S703*-0906	Tpwv	1.5	2	-	µs
		S703*-0907/-1006		3	4	-	
		S703*-1007		6	8	-	
	Rise and fall times		Tprv, Tpfv	10	-	-	ns
P1H, P2H*1	Pulse width		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG–P1H	Overlap time		Tovr	3	-	-	µs

*1: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

[Figure 1-55] Timing chart of two-dimensional operation

(a) Low dark current mode



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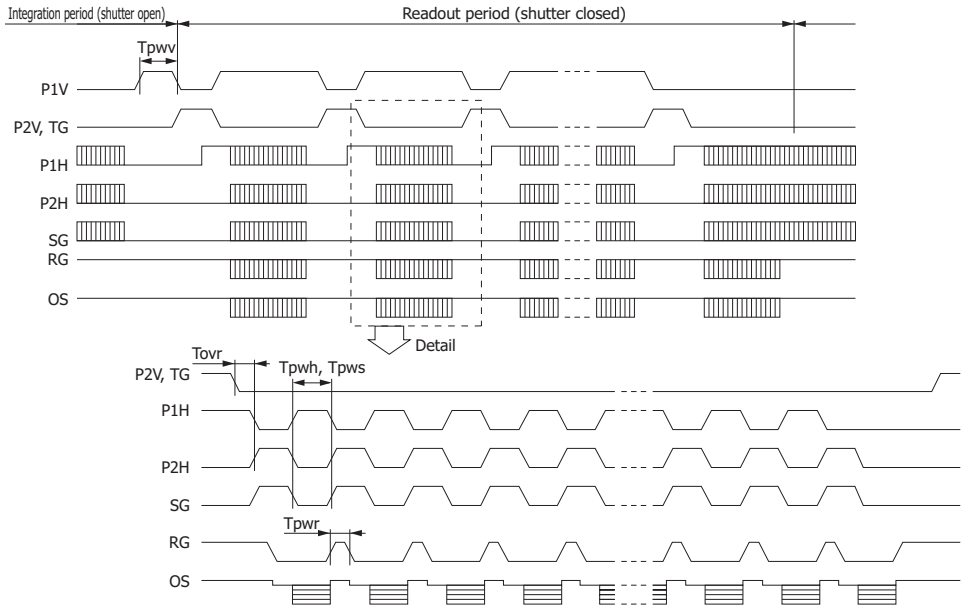
(b) Large saturation charge mode



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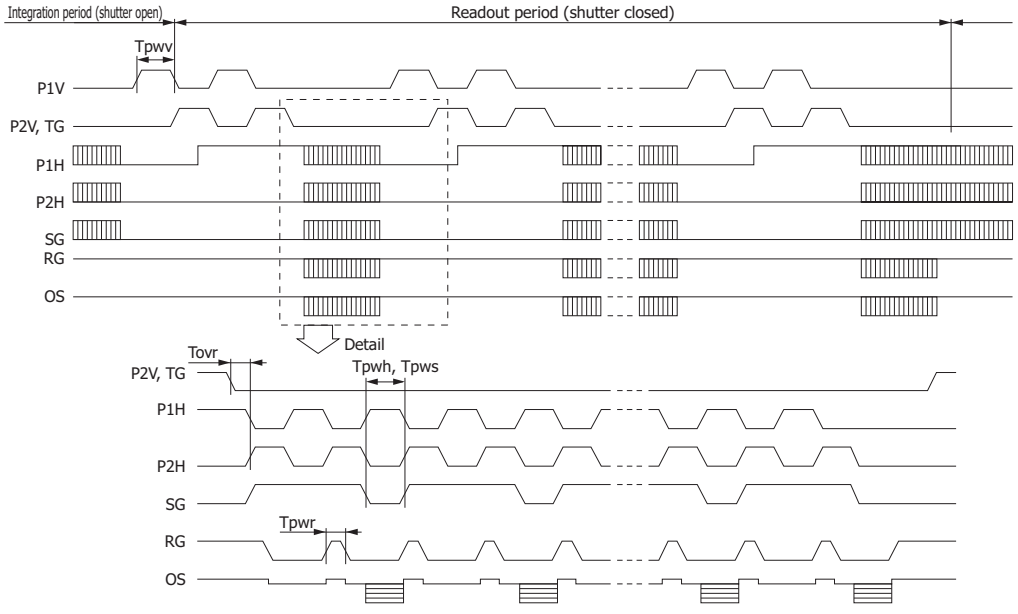
Parameter		Sensor	Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width*2	S7171-0909-01	Tpwv	6	8	-	μs
	Rise and fall times	All series	Tprv, Tpfv	200	-	-	ns
P1H, P2H	Pulse width*2		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	40	50	60	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	40	50	60	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time		Tovr	3	-	-	μs

*2: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

[Figure 1-56] Timing chart of pixel binning (2 × 2)

(a) Low dark current mode



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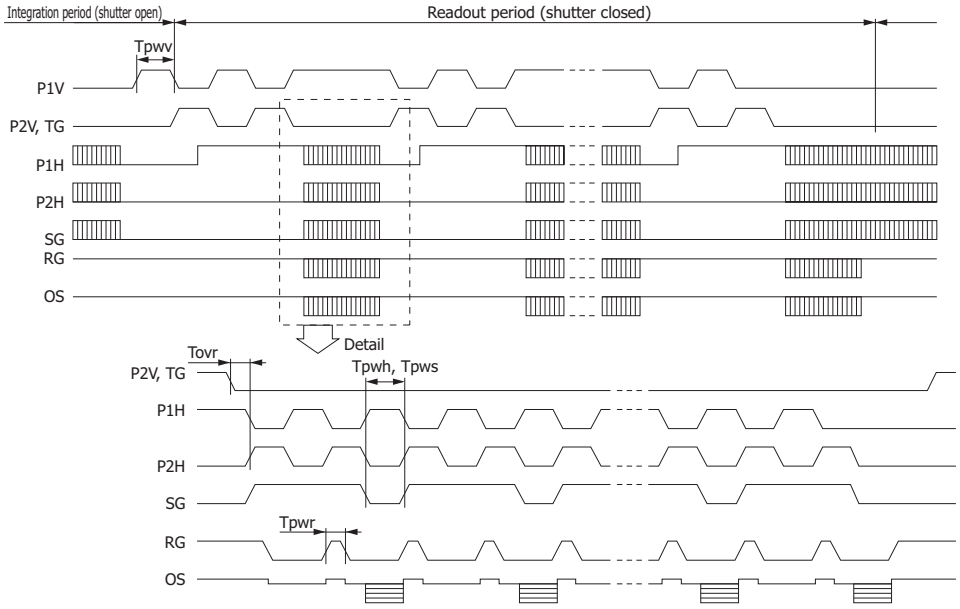
(b) Large saturation charge mode



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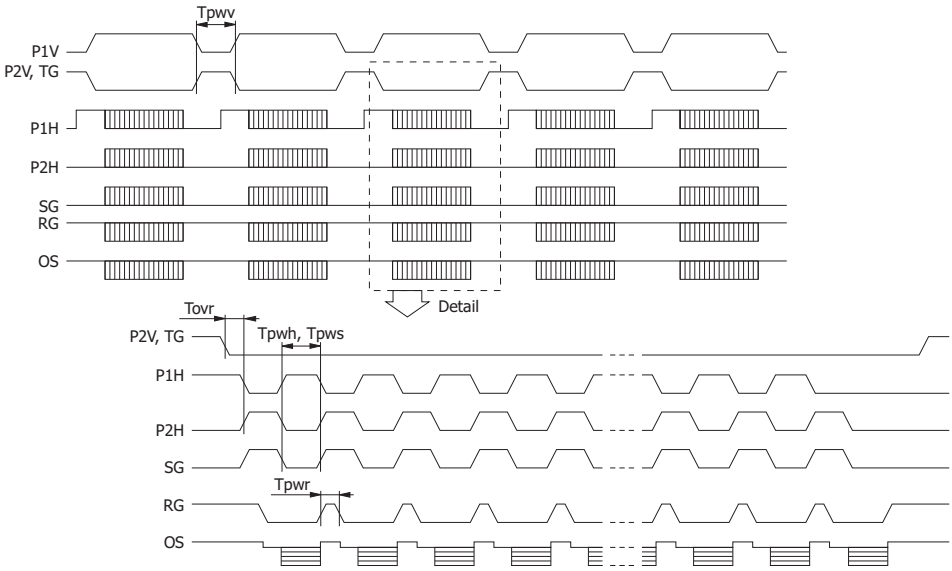
Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*1	Pulse width	S703*-0906	Tpwv	1.5	2	-	µs
		S703*-0907/-1006		3	4	-	
		S703*-1007		6	8	-	
	Rise and fall times		Tprv, Tpfv	10	-	-	ns
P1H, P2H*1	Pulse width		Tpwh	500	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	500	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	100	-	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG–P1H	Overlap time		Tovr	3	-	-	µs

*1: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

[Figure 1-57] Timing chart of TDI operation

(a) 1 × 1



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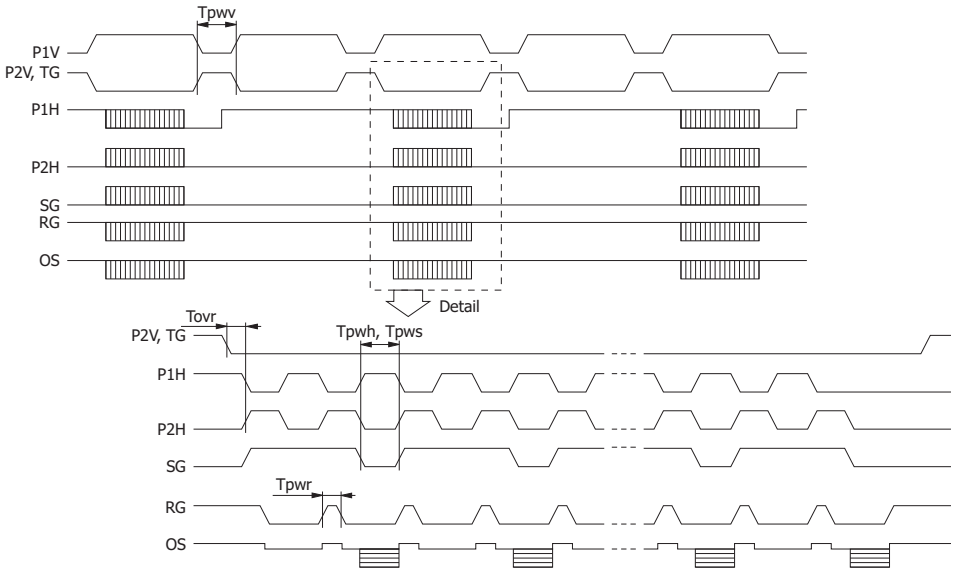
Note: For the timing chart in low dark current mode, see P1V, P2V, and TG in Figure 1-55 (a).

(b) 2 × 2, pixel binning



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Note: For the timing chart in low dark current mode, see P1V, P2V, and TG in Figure 1-56 (a).

Parameter		Sensor	Symbol	Min.	Typ.	Max.	Unit
P1AV, P1BV P2AV, P2BV, TG*2 *3	Pulse width	S7199-01	tpwv	30	-	-	µs
	Rise and fall times		tprv, tpfv	200	-	-	ns
P1AH, P1BH P2AH, P2BH*3	Pulse width		tpwh	125	-	-	ns
	Rise and fall times		tprh, tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		tpws	125	-	-	ns
	Rise and fall times		tprs, tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		tpwr	10	-	-	ns
	Rise and fall times		tprr, tpfr	5	-	-	ns
TG-P1AH, P1BH	Overlap time		tovr	10	-	-	µs

*2: Apply the same pulse as P2AV to TG.
*3: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

(2) Two-dimensional operation (area scan)

This operation transfers all horizontal signal charges each time one bit is transferred in the vertical direction. When the transfer in the vertical direction is fully complete, a frame transfer is complete. At this point, the summing gate pulse should be set exactly as the clock pulse (P2H) for the horizontal shift register.

(3) Pixel binning

One bit is first transferred in the vertical direction. Then all the horizontal signal charges are transferred. At this point, by halting the summing gate pulses for the number of bits required for summing, the signal charges are added to the summing well.

Note: Line binning and pixel binning can be performed at the same time.

(4) TDI operation

As explained in "TDI-CCD" in section 1-1, "Structure and operating principle," TDI operation allows imaging of a moving object. To do this, the CCD vertical transfer clock pulse must be synchronized with the speed at which the object moves along the photosensitive area surface of the CCD.

Clock pulse and DC bias adjustment

The clock pulse and DC bias must be adjusted properly to make fullest use of CCD performance.

(1) Transfer clock pulse

The low level of the clock voltage for the vertical shift register affects the CCD dark current. If it is set to a voltage higher than the pinning voltage that initiates MPP operation, the dark current will not lower as expected. The pinning voltage differs according to the individual CCD due to variations in device production. Ideally, it should be adjusted for each product.
After determining the low level of the vertical clock voltage, adjust the high level. The clock pulse amplitude should be large enough to maintain the desired is set too large, the spurious charges become large, causing the dark current (Nb) during the readout time to increase and resulting in an offset that appears in the entire output signal. Normally, the spurious charges cannot be distinguished from the dark current at around room temperature, but they may cause problems when the CCD is cooled. Therefore, the vertical clock pulse amplitude should be adjusted to a minimum as long as other characteristics are not impaired.

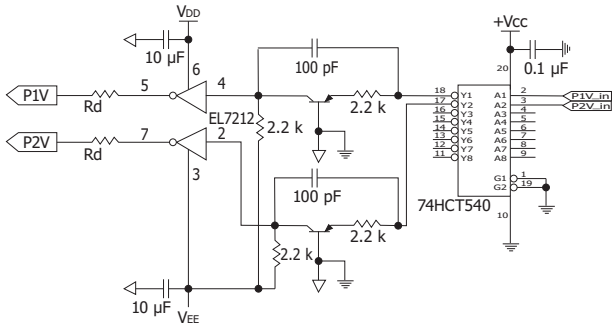
(2) Reset clock pulse

The reset clock pulse is applied to the reset gate (RG) to periodically reset the signal charge flowing into the FD (floating diffusion) to the reference voltage (V_{RD}). Adjusting the low and high levels of this clock pulse changes the saturation charge level of the output section. When these are properly adjusted, the saturation charge level of the output section is sufficiently larger than the CCD saturation charge. If the low level voltage of the reset clock pulses becomes high, the charge that can be stored in the FD decreases because the potential has not lowered sufficiently in a state where the reset switch is off. This may cause an overflow before all transfer charges are converted into voltage. For this reason, the low level of the reset clock pulses must be set to a voltage low enough not to affect the saturation charge level of the output section.
Set the pulse width of the reset clock pulses to about 10 ns to 100 ns (there will be no problem if longer than 100 ns).

(3) Transfer clock pulse generator

Figure 1-58 shows an example of a transfer clock pulse generator. As stated above, clock pulses with high and low levels of voltage amplitude are required to operate a CCD. These clock pulses must drive the vertical shift register and horizontal shift register at high speeds, which have an input capacitance of several hundred picofarads to several nanofarads. For this purpose, MOS driver IC is commonly used to drive a CCD since it is capable of driving a capacitive load at high speeds.
Normally, the timing signal generator circuit uses a TTL or CMOS logic level IC. The operating voltage for these ICs is +3.3 V or +5.0 V, so a level converter circuit must be connected to the MOS driver IC.
In 2-phase CCD operation, the clock pulses for driving the vertical and horizontal shift registers must overlap with each other (see "Charge transfer operation" in section 1-1, "Structure and operating principle"). For this reason, a resistor Rd with an appropriate value (damping resistor: a few to several dozen ohms) should be placed between the MOS driver IC and the CCD in order to adjust the rise time and fall time of the clock pulses.
To minimize noise intrusion to the CCD from digital circuits, it is recommended that the analog ground and digital ground be set to the same potential by the transfer clock pulse generator.

[Figure 1-58] Example of transfer clock pulse generator



V_{DD}: high level voltage of clock pulse
V_{EE}: low level voltage of clock pulse
Rd: damping resistor (a few to several tens of ohms)

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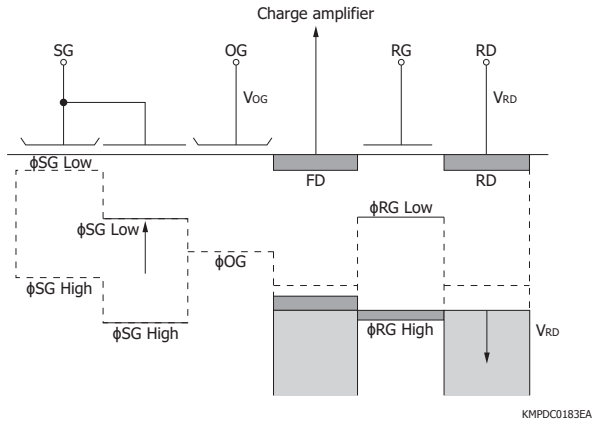
[Figure 1-59] Potentials in CCD output section



(4) DC bias

• Bias (V_{OD}) applied to OD

V_{OD} is the bias voltage applied to the output transistor. When using a one-stage source follower output amplifier, apply approx. 20 V as V_{OD}. In a source follower circuit using a load resistance of about 20 kΩ connected to the MOSFET source, the source DC level is about 15 V. Therefore, although several volts are applied across the source and drain of the MOSFET via the voltage applied to the OD, the following phenomena will occur unless this voltage is sufficiently high.

① Voltage gain (Av) in the source follower circuit is lowered.
② MOSFET does not operate in the saturation region.

These phenomena adversely affect CCD performance. For example, they may cause a decrease in the conversion factor (unit: μV/e⁻), an increase in the readout noise, or deterioration in the linearity.
When using a multi-stage amplifier such as a two-stage source follower output type, set V_{OD} to approx. +15 V, which is lower than V_{OD} for a one-stage type. As in the case of one-stage type, phenomena ① and ② occur in the two-stage source follower output type.

• Bias (V_{RD}) applied to RD

V_{RD} is the bias voltage applied to the reset drain. It determines the reset level of the output section and also serves as the gate voltage of the output transistor. The V_{RD} determines the voltage gain and MOSFET operating region the same as with V_{OD} and also affects the saturation charge level of the output section. Increasing the V_{RD} also raises the potential in the FD and the amount of signal increases. However, it must be set to an optimum value in consideration of phenomena ① and ② which may occur in the output transistor.

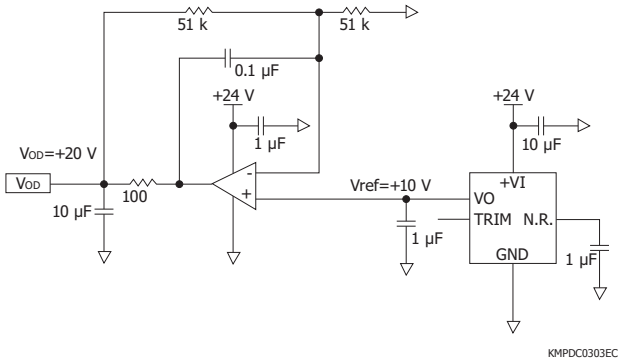
• Bias (V_{OG}) applied to OG

V_{OG} is the bias voltage applied to OG that separates the FD arranged at the last stage of the horizontal shift register from the last clocking gate (summing gate). The signal charge is output to the FD in synchronization with the falling edge to the low level of the summing gate pulse (SG) which is the last clocking gate. The OG potential therefore becomes smaller than the SG potential at low level, and the difference between the OG potential and the potential at reset becomes the factor that determines the amount of signal charge that can be handled. As seen from Figure 1-59, the amount of signal charge is limited by either the potential under OG or the potential of the reset gate at low level. As V_{OG} decreases, the saturation charge level of the output section increases. If V_{OG} is too low, however, the signal charge is unable to flow into the FD during the low level of SG, so V_{OG} must be adjusted to an appropriate value.

• Bias voltage generator circuit

The bias voltage is mainly applied to the peripheral section of the CCD output amplifier, so use a stable power supply with relatively low noise. It is also important to note the voltage accuracy, voltage fluctuation, ripple, and output current.
Figure 1-60 shows an example of a bias voltage generator circuit for the OD terminal. The reference voltage is generated from the power supply IC and is set to a specified voltage value by the amplifier making up the low-pass filter. This allows obtaining a highly stable and accurate voltage with low noise.

[Figure 1-60] Example of bias voltage generator circuit

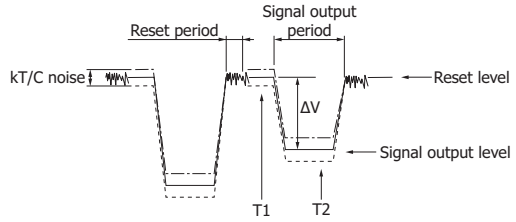


Signal processing circuit

Major sources of noise from a CCD are the well-known kT/C noise and 1/f noise. The kT/C noise is generated by a discharge (reset operation) in the FDA (see "FDA" in section 1-1, "Structure and operating principle"). This noise is inversely proportional to the square root of the node capacitance (Cfd) of the FDA and makes up a large percentage of the total noise of a CCD. The 1/f noise is generated by the MOSFET constituting the FDA and is inversely proportional to the frequency.
These noises degrade the S/N in the CCD system and therefore should be reduced as much as possible in the signal processing circuit. A typical circuit for this purpose is a CDS circuit.
The operating principle of the CDS circuit is described below. Figure 1-61 shows an output waveform from a CCD. As stated above, kT/C noise occurs during a reset period in the FDA. At the point where the reset period has ended, the voltage level varies due to kT/C noise. Therefore, if data is acquired at time T2, the S/N deteriorates by an amount equal to the kT/C noise variation. In contrast,

acquiring data at times T1 and T2 on the output waveform and then obtaining the difference between them will extract only a signal component ΔV with the kT/C noise removed. DC components such as the offset voltage component and reset feed-through are removed at the same time.

[Figure 1-61] CCD output waveform



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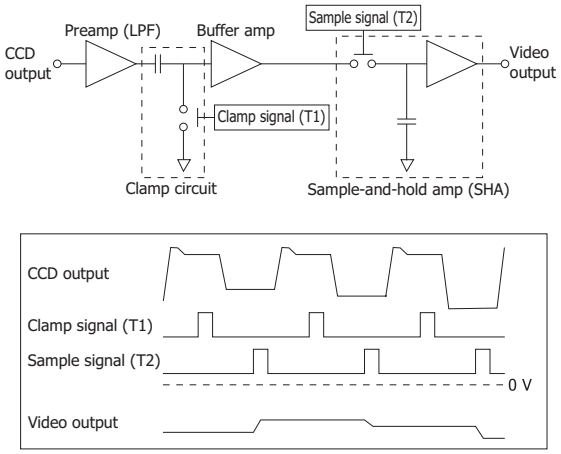
There are two types of CDS circuits: "Type 1" that uses a clamp circuit in combination with a sample-and-hold amplifier (SHA), and "Type 2" that uses a SHA in combination with a differential amplifier. Type 1 has a very simple circuit configuration [Figure 1-62]. But if the ON resistance of the switch used in the clamp circuit is large, the amount of noise that can be removed will be small or a DC voltage error will occur. Ideally, the ON resistance should be 0 Ω.

[Figure 1-62] CDS circuit block diagram (using clamp circuit and SHA)



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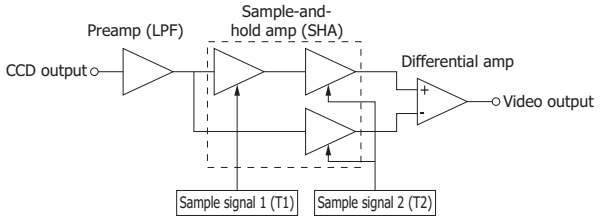
Type 2 [Figure 1-63] uses a larger number of components but removes noise more effectively than Type 1. However, since Type 2 makes an analog calculation of the SHA output, the noise of the SHA itself may be added, resulting in increased noise in some cases. The SHA noise should be small enough so that the kT/C noise can be ignored.

[Figure 1-63] CDS circuit block diagram (using SHA and differential amplifier)



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A circuit example of Type 1 is shown in Figure 1-64.
The preamp gain should be set high in order to sufficiently amplify the CCD output signal. Since the CCD output signal contains DC voltage components, a capacitor is used for AC coupling. Note that this capacitor can cause a DC voltage error if the preamp bias current is large. Therefore, a preamp with a small bias current must be selected. A JFET or CMOS input amplifier is generally used. It is also necessary to select a low-noise amplifier with a bandwidth wide enough to amplify the CCD output waveform.
The clamp circuit is made up of capacitors and an analog switch. For the analog switch, we recommend using a high-speed type having low ON resistance and small charge injection amount.
For the preamp, the last-stage amplifier is AC-coupled via a capacitor, so a JFET or CMOS input amplifier should be selected. In addition, a non-inverted amplifier must be configured to allow high input impedance.
Incidentally the CCD provides a negative-going output while the last-stage amplifier gives a positive-going output to facilitate analog-to-digital conversion. For this reason, an inverted amplifier is connected after the preamp.

High-speed signal processing circuit

For a CCD signal processing circuit that requires high-speed readout at several megahertz or faster, it is difficult for a circuit constructed only of discrete components to achieve high-speed clamp operation and fast capacitor charging/discharging response.
A high-speed signal processing circuit can be constructed by using an analog front-end IC (a single IC chip consisting of CDS, gain, and offset circuits, A/D converter, etc.) optimized for CCD signal processing.

Measures against light emission on the output circuit

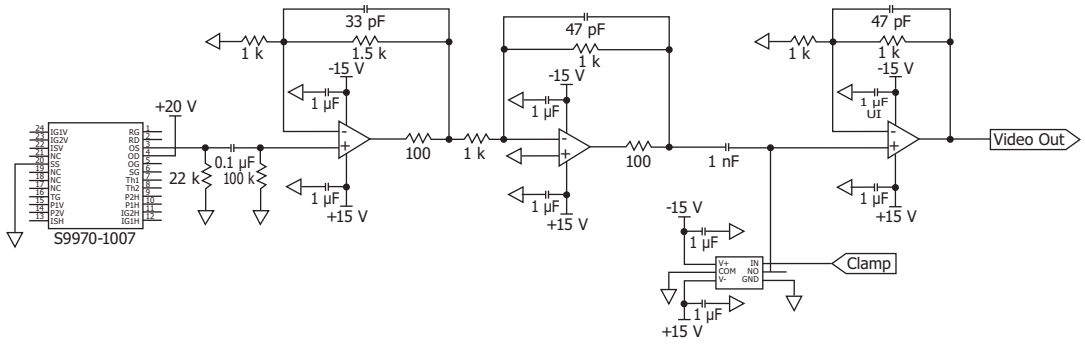
If the operating conditions are not suitable for the CCD output circuit employing a two-stage MOSFET source follower, the amplifier may emit light. If this light is received by the resistive gate, storage gate, or horizontal shift register, the output for the first pixel that is read out will be large even in a dark state [Figure 1-67].
To reduce this effect, the following measure is effective.

① Apply +1 V typ. to the Vret terminal (if a Vret terminal is available).

② Intersect the horizontal shift register clock pulse (P1H, P2H) at the amplitude of 50% ± 10% [Figure 1-68].
· Horizontal 2-phase drive: P1H, P2H
· Horizontal 4-phase drive: P1H, P3H and P2H, P4H

③ After reading out all pixels, perform horizontal dummy readout up to immediately before TG is set to high level.

[Figure 1-64] CDS circuit example (using clamp circuit and SHA)



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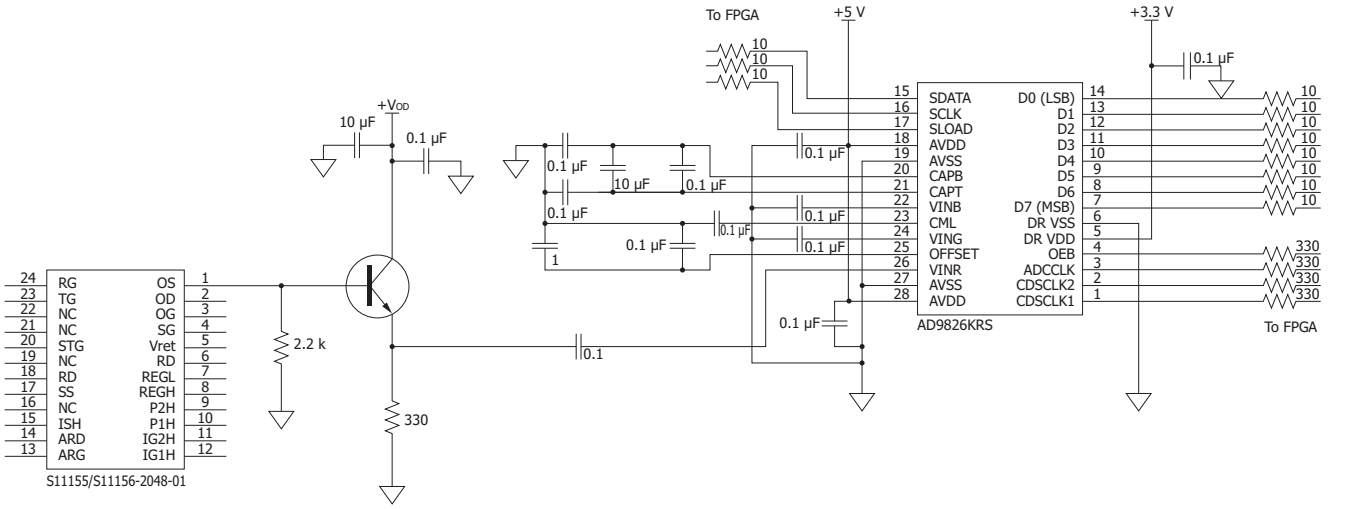
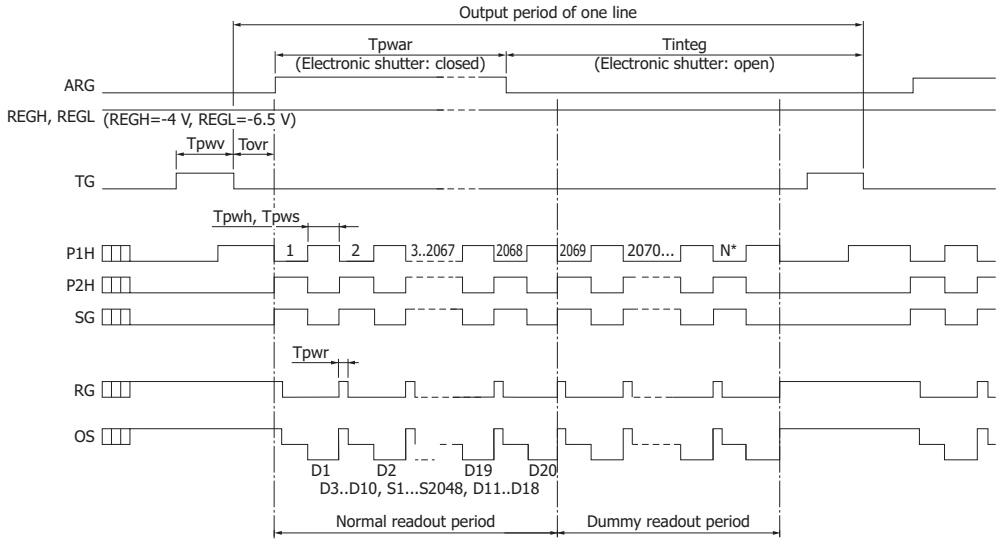
[Figure 1-65] High-speed signal processing circuit example (using S11155/S11156-2048-01 and analog front-end IC)



KMPDC0457EB

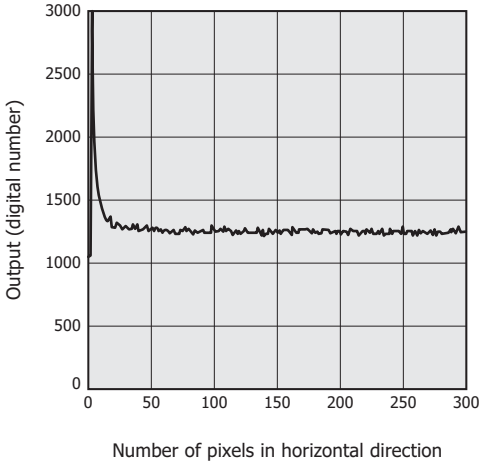
[Figure 1-66] Timing chart (S11155-2048-01)



* Apply clock pulses to appropriate terminals during dummy readout period.
Set the total number N of clock pulses according to the integration time.

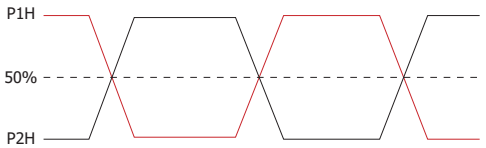
KMPDC0382EC

[Figure 1-67] Effect of light emission on the output circuit (horizontal profile in a dark state, typical example)



KMPDB0328EA

[Figure 1-68] Waveform of horizontal shift register clock pulses



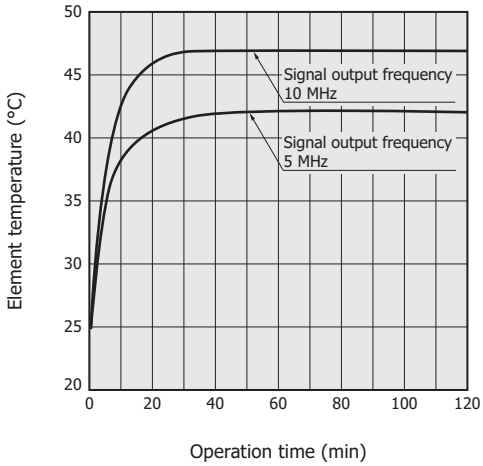
KMPDC0381EA

When integrating over a relatively long period, to discard the charge generated by the horizontal shift register, after reading out all pixels, a dummy readout is performed up to immediately before beginning the transfer to the transfer gate. This method is effective also when discarding the charge generated by the horizontal shift register during the integration time.

Element temperature

Figure 1-69 is a measurement example showing the relationship between the element temperature and operation time when the S11155-2048-01 is operated using our evaluation circuit (the circuit system is sealed and without any heat dissipation measures). The element temperature increases significantly when operated at high speeds. Since an increase in element temperature causes an increase in dark current, it is recommended that heat dissipation measures be taken such as by providing a heatsink or a fan.

[Figure 1-69] Element temperature vs. operation time (S11155-2048-01, using our evaluation circuit, typical example)



KMPDC0382EA

Correction

Image sensors generally have two nonuniformities: 1) photoresponse nonuniformity (PRNU) that is variations in sensitivity to photons between pixels, and 2) dark current nonuniformity (DCNU) that occurs under the set operating conditions. At least these two nonuniformities must be corrected to collect highly accurate data. Since these nonuniformities vary with temperature, the correction must take the temperature into account.

(1) Dark current correction

Dark current differs from pixel to pixel and must therefore be handled at the pixel level to make accurate corrections. When no light is incident on the CCD, the dark current (Nt) is expressed by equation (16).

$$Nt(x, y, t, T) = Nd(x, y, T) \times t + Nb(x, y, T) \cdots\cdots (16)$$

x : horizontal direction address
y : vertical direction address
t : integration time
T : CCD temperature
Nd(x, y, T): dark current of each pixel [e^-/pixel/s]
Nb(x, y, T): dark current when integration time is zero

When the integration time is zero, the dark current Nb(x, y, T) is also called the offset or bias. This value varies with the operating conditions. The dark current values listed in our datasheets are the dark currents of Nd(x, y, T) averaged over a certain region and are different from the dark current actually output from the CCD. To correct the dark current, both Nd and Nb must be acquired. Nd and Nb can be acquired from a single data readout, but more accurate correction image data that excludes the effect of disturbing noise can be obtained by acquiring a few or up to a dozen images and taking their average.

(2) Flat field correction

As described in “Photoresponse nonuniformity” in section 1-2 “Characteristics,” the sensitivity of each pixel in a CCD is not uniform, so it must be corrected at the pixel level just as with the dark current. An uncorrected output I(x, y)

measured under certain exposure conditions is given by equation (17).

$$I(x, y) = Nt(x, y, t, T) + i(x, y) \times r(x, y) \cdots\cdots\cdots (17)$$

i (x, y): original image output
r(x, y): sensitivity of each pixel

To acquire the original image output i(x, y), not only the dark current (Nt) but also r(x, y) must be known. Normally, the sensitivity r(x, y) can be acquired by illuminating a CCD with extremely uniform light and measuring the output. However, uniformly illuminating the entire surface of a CCD is difficult. Moreover, the sensitivity may vary with wavelength depending on the position of the CCD photosensitive area. To accurately correct this within 1% or less, it is necessary to acquire correction data while paying attention to the optical systems and temperature, etc. The sensitivity r(x, y) can be acquired from a single data readout, but more accurate calibration data can be obtained by acquiring a few or up to a dozen images and taking their average to eliminate the effect of external noise.

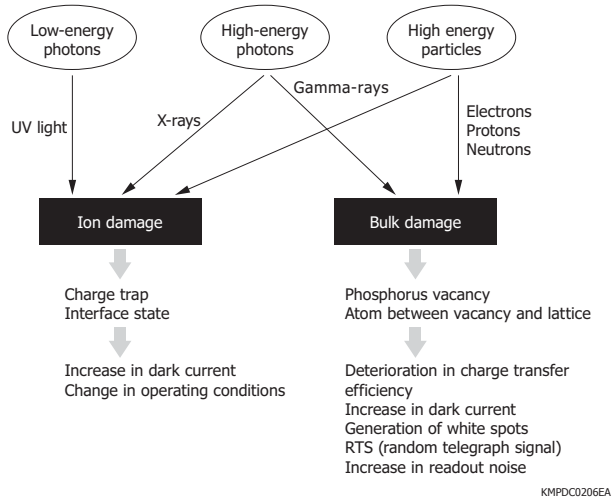
Coupling to FOS

Coupling an FOS (fiber optic plate with scintillator) to a front-illuminated CCD allows detecting X-rays up to several dozen keV or higher. See section 3 “CCD area image sensors” in chapter 9 “X-ray detectors” for more information.

Damage by radiation

Ion damage and bulk damage can occur in a CCD due to radiation, the same as with other devices made of silicon. This must be considered before attempting to use a CCD for X-ray detection or in space environments.

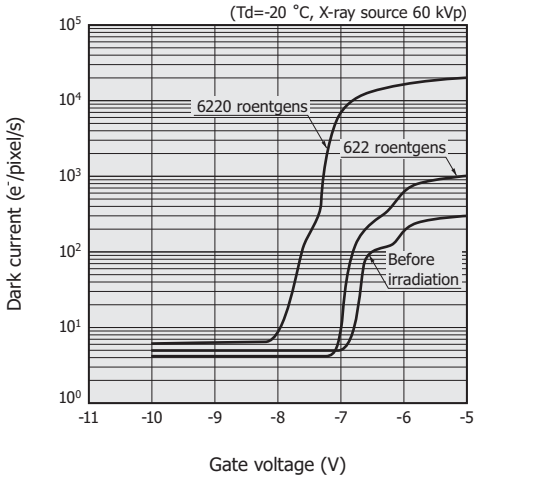
[Figure 1-70] Effects of radiation on CCDs



Ion damage occurs when photons with energy higher than a certain level (energy levels roughly higher than ultraviolet light) enter a CCD and the resulting electron-hole pairs are generated in the gate oxide film. Most electron-hole pairs generated by photons will recombine and disappear. However, some of the holes with less mobility than electrons are trapped in the oxide film and produce a voltage that can shift the CCD operating gate voltage. This causes the CCD pinning voltage to shift toward the negative side (amount of shift may be up to several volts in some cases). When high energy electrons or photons enter, both ion damage and bulk damage occur. On the other hand, heavy particles such as protons and neutrons also generate charges in the gate insulation film. Electrons and photons generate a new interface state at the oxide film interface. Since the energy level of that new interface state is within the band gap, the dark current will increase.

Bulk damage occurs when energized charged particles like protons interact with the silicon atoms. If protons have enough energy, they displace the silicon atoms from their lattice positions to interstitial locations (energy of approx. 100 eV is required to cause this). The displaced silicon atoms then collide with other silicon atoms to further displace more atoms. The resulting defects serve as electron traps. If many electron traps are created inside the charge transfer channels of the CCD, the charge transfer efficiency (CTE) will deteriorate. Those defects will become pixels with a large dark current.

[Figure 1-71] Damage by X-rays (S9970-0907, typical example)

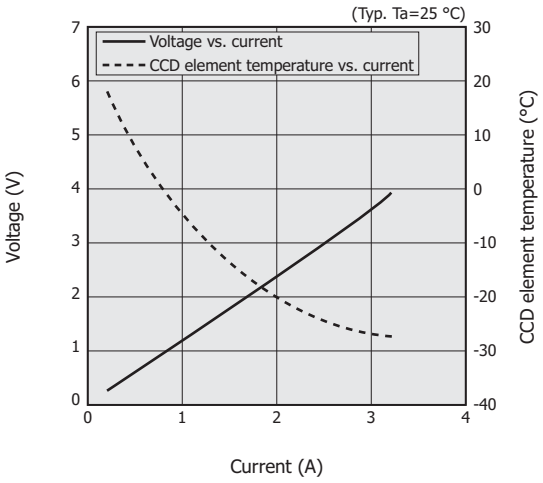


Heat dissipation

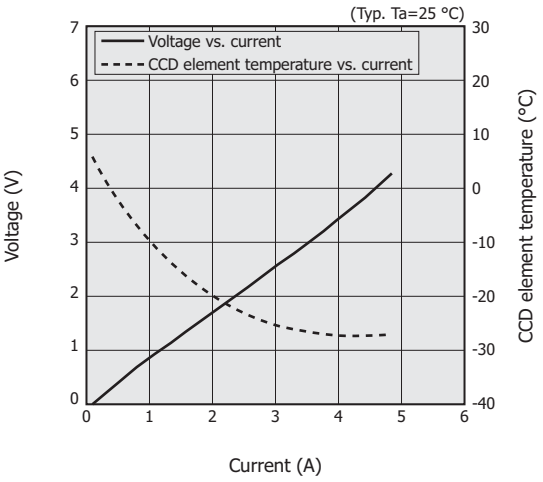
(1) Heatsink selection

When using a thermoelectrically cooled CCD, you must select a heatsink with sufficient heat dissipation capacity.

[Figure 1-72] Temperature characteristics of one-stage thermoelectrically cooler (S7031-1006S/-1007S, CCD undriven)



[Figure 1-73] Temperature characteristics of two-stage thermoelectrically cooler (S7032-1007, CCD undriven)



(2) Device design

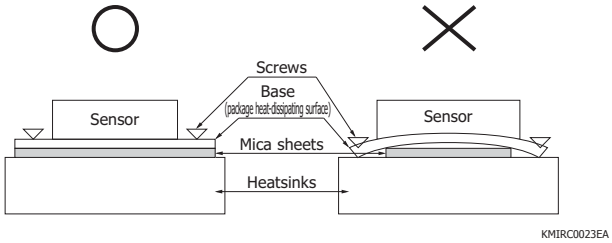
The device must be designed so that the heat generated by the heatsink is adequately dissipated. Provide good air ventilation by installing air fans and ventilation ducts.

(3) Heatsink mounting method

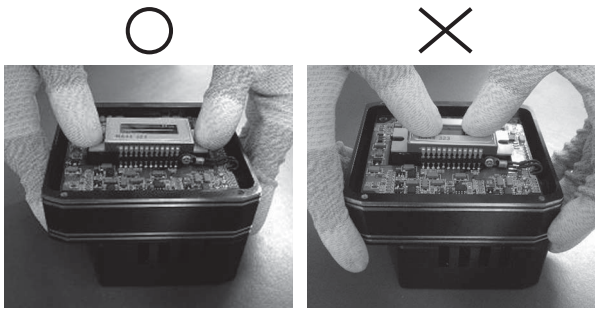
To allow the thermoelectric cooler to exhibit fullest cooling capacity, the heatsink must be mounted correctly onto the product. Mount the heatsink while taking the following precautions.

- Check that the heat-dissipating surface of the product and the attachment surface of the heatsink are clean and flat.
- If the heat dissipation by the thermoelectric coolers during cooling is insufficient, the element temperature will increase and may cause physical damage to the product. Provide sufficient heat dissipation during cooling. As a heat dissipation method, we recommend inserting a highly thermal conductive material (e.g., thermally conductive silicone gel GR-d by Fuji Polymer Industries, thermally conductive silicone SE 4490 CV by Dow Corning Corporation, thermally conductive sheet 5580H by 3M) between the product and heatsink. Such material should be applied over the entire junction area of the product and heatsink with uniform thickness. When a mica sheet is used, it must also make contact with the entire heat-dissipating surface of the package. The cooling effect will degrade if the sensor package is fastened to the heatsink with screws while the mica sheet is still too small to cover the screw positions. This may also warp the package base, causing cracks between the sensor and the package base [Figure 1-74].
- Never press the window when inserting the product into the circuit board. Pressing the window may crack or break the window or cause the window to fall out, resulting in a malfunction [Figure 1-75].
- When fastening a heatsink to the product with screws, set the tightening torque to 0.3 N·m or less, and tighten the two screws alternately to apply uniform stress on the product.

[Figure 1-74] Method of mounting to heatsink



[Figure 1-75] Method of mounting to circuit board



(4) Current supplied to thermoelectric cooler

To protect the thermoelectric cooler and to maintain stable operation, set the current supplied to the thermoelectric cooler to no greater than 60% of the maximum current specified in the datasheet.

Electrostatic and surge measures

CCDs may become damaged or deteriorate if subjected to static electrical charges and voltage surges. Take the following precautions to avoid trouble.

(1) Handling precautions

When taking a CCD out of the packing box, always do so in locations where anti-electrostatic measures are provided. For example, lay a grounded conductive sheet (1 MΩ to 100 MΩ) on the work bench or work floor.
When handling CCD sensors, always wear a wrist strap

and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.
Always ground the soldering iron so no leakage voltage is applied to the device.
Do not bring charged objects (VDT for a PC or insulator materials such as plastics and vinyl) close to the CCD. The CCD may become electrically charged just by being brought close to a charged object, causing ESD (electrostatic discharge) damage.

(2) Usage precautions

Measurement devices and jig tools must be properly grounded so no surges are applied to the CCD by a leakage voltage. Do not allow a voltage exceeding the absolute maximum rating to be applied to the CCD from the measurement device or tester, etc. (This tends to occur during ON/OFF switching of power sources, so use caution.)
If there is the possibility of a surge voltage, insert a filter (made up of a resistor or capacitor) to protect the CCD.
When installing the CCD, be extremely careful to avoid reverse insertions, wrong insertions, or shorts between terminals.
Do not attach or detach any connector that is connected to the power supply line or output line during operation.

(3) Carrying precautions

When carrying a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting leads) and then put it in a conductive case. The PC board for mounting the CCD should also be put in a conductive case for carrying. Avoid using plastic or styrofoam boxes since they may generate static electricity due to vibration during shipping and cause device deterioration or breakdowns.

(4) Storage precautions

When storing a CCD, place it on a conductive mat by inserting the lead pins into the mat (for shorting the leads) and then put it into a conductive case. The PC board for mounting the CCD should also be put in a conductive case.
Avoid placing CCDs near equipment that may generate high voltage or high magnetic fields.

It is not always necessary to provide all the electrostatic and surge measures stated above. Implement these measures according to the extent of deterioration or damage that may occur.

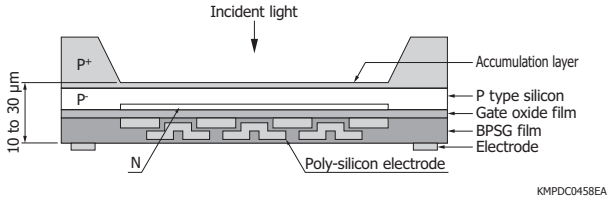
1 - 4 New approaches

Hamamatsu will continue to develop new CCDs by applying new technologies in addition to the technologies accumulated in the past.

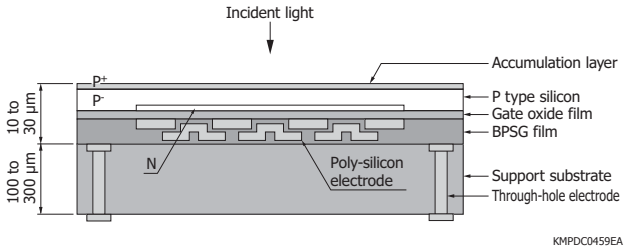
(1) Fully thinned CCD

Except for a portion of the near infrared-enhanced types, our back-thinned CCDs are partially thinned types in which a portion of the silicon is made thin. Since the silicon thickness of the photosensitive area of partially thinned CCDs is approximately 10 to 30 µm, it is difficult to fabricate large-area devices. In addition, because the thin silicon must be enclosed with thick silicon to provide support, it is difficult to fabricate light-shielding parts or mount FOP on the photosensitive surface.
To solve these problems, Hamamatsu is developing fully thinned CCDs. To create a fully thinned structure, a supporting substrate is pasted to the wafer and then the entire wafer is made thin. Through-hole electrodes are fabricated on the supporting substrate side. The adoption of this fully thinned structure strengthens the chip and makes fabrication of large-area devices possible. This also makes it easy to form light-shielding parts and mount FOP on the photosensitive surface.

[Figure 1-76] Structure of partially thinned CCD



[Figure 1-77] Structure of fully thinned CCD



(2) TDI-CMOS CCD

The TDI-CMOS CCD is an image sensor that combines the feature of the TDI-CCD that allows acquiring of high S/N images even under low-light conditions during high-speed imaging and the features of the CMOS sensor that provides digital output (an A/D converter is built into the chip) and low voltage operation. Signal charges are integrated and transferred in the charge state through TDI operation, converted into voltage by a readout amplifier in each column, converted into a digital signal by the on-chip signal processing circuit and A/D converter, and then output.

(3) Back-thinned CCD with suppressed UV-light-irradiation-caused sensitivity deterioration

We are developing back-thinned CCDs with high sensitivity in the ultraviolet region and low sensitivity deterioration (deterioration becomes a problem during UV light irradiation) by applying ingenuity to the production method and sensor structure.

2. NMOS linear image sensors

NMOS linear image sensors are self-scanning photodiode arrays designed as detectors for multichannel spectrophotometers. The scanning circuit of these image sensors is made up of N-channel MOS transistors and operates at low power consumption, making them easy to use. Each photodiode has a large photosensitive area and high UV sensitivity, yet the noise is extremely low so high S/N signals can be obtained even at low light levels. Current output type NMOS linear image sensors also deliver excellent output linearity and wide dynamic range.

2 - 1 Features

- Wide photosensitive area
- High UV sensitivity and stable characteristics under UV light irradiation
- Low dark current and large saturation charge

  Allows a long integration time and wide dynamic range at room temperature
- Excellent output linearity and sensitivity uniformity
- Low power consumption
- CMOS logic compatible start pulse and clock pulse
- Infrared-enhanced type: high sensitivity in infrared and soft X-ray regions
- Thermoelectrically cooled type: highly reliable package sealed with sapphire window

2 - 2 Structure

NMOS linear image sensors consist of a photodiode array that performs photoelectric conversion and stores the resulting charges, address switches connected to each photodiode, and a digital shift register. Each address switch

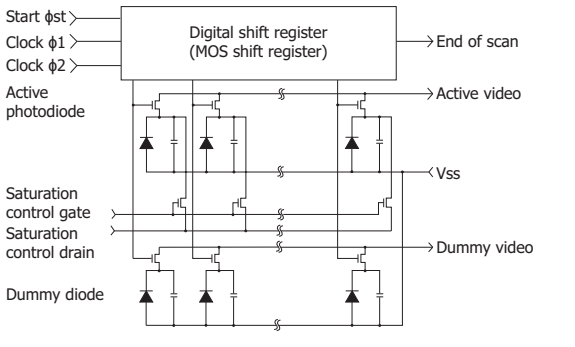
[Table 2-1] Hamamatsu NMOS linear image sensors (current output type)

Type	Type no.	Pixel height (mm)	Pixel pitch (μm)	Number of pixels
Standard type	S3901 series	2.5	50	128, 256, 512, 1024
	S3904 series		25	256, 512, 1024, 2048
	S3902 series	0.5	50	128, 256, 512
	S3903 series		25	256, 512, 1024
Infrared-enhanced type	S8380 series	2.5	50	128, 256, 512
	S8381 series		25	256, 512, 1024

Note: We also offer voltage output types with built-in current integrating circuit and thermoelectrically cooled types for low-light-level detection.

is a MOS switch with the source connecting to a photodiode, the gate handling the address pulses from the shift register, and the drain connecting to the video line (common output line). Figure 2-1 shows an equivalent circuit of a current output type NMOS linear image sensor (S3901 to S3904 series).

[Figure 2-1] Equivalent circuit (S3901 to S3904 series)



2 - 3 Operating principle

Photodiodes are initialized to a certain potential from an external circuit when their address switches turn on. When light enters a photodiode, a photocurrent proportional to the incident light level flows in the photodiode, and a charge (Qout = I_L × Ts) equal to the product of the photocurrent (I_L) and the integration time (Ts) is stored in the junction capacitance (Cj) of the photodiode. The integration time is the period between the times that the photodiode address switch turns on. It corresponds to the time interval between the start pulses applied to the shift register. This photodiode operation is called the charge integration mode and allows acquiring a large signal even from image sensors with small pixels by integrating the charge. In low-light-level detection, making the integration time longer yields a large output.

The shift register starts scanning when a start pulse is input with a clock pulse train applied to the shift register. The address switch connected to the first pixel photodiode first turns on in synchronization with the clock pulse and the charge stored in the first pixel photodiode is output to the external circuit via the video line. The first pixel address pulse then turns off, and the second pixel address pulse turns on, allowing the charge stored in the second pixel photodiode to be read out to the external circuit in the same way. By sequentially repeating this operation until the last pixel is scanned, the position information of light irradiated onto the linearly arranged photodiode array is read out to the external circuit as time-series signals including a time differential.

The minimum integration time is the product of the readout time per pixel and the number of pixels. In NMOS linear image sensors, the address switch on/off operation determines the integration time of the photodiode, and its timing shifts for each photodiode. So even though the integration time is the same for all pixels, the integration start time and end time for each pixel will differ. The next start pulse cannot be input until the last pixel is scanned.

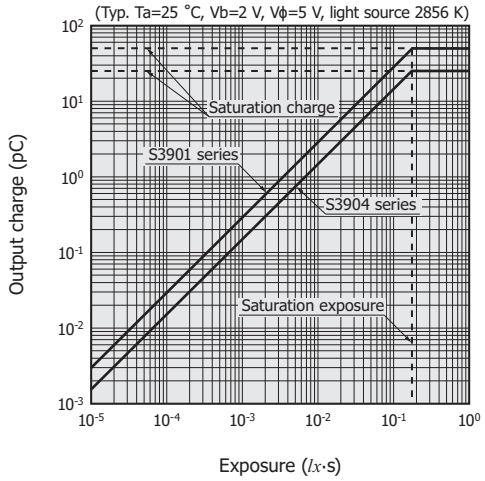
2 - 4 Characteristics

Input/output characteristics

Figure 2-2 shows input/output characteristics of current output type NMOS linear image sensors (S3901/S3904 series). The horizontal axis indicates the exposure amount which is the product of the incident light level and the integration time. Since no photodiode can store a charge larger than its junction capacitance × bias voltage, there is an upper limit on the output charge. This upper limit on the output charge is referred to as the saturation charge, and the exposure at this point is referred to as the saturation exposure.

In an over-saturated state, an excess charge flows into the overflow drain connected to the photodiode and will not affect other pixels. When a charge amplifier is used to read out the signal, the actual output deviation from the ideal line γ=1 is within 1% which indicates satisfactory input/output characteristics.

[Figure 2-2] Output charge vs. exposure (S3901/S3904 series)



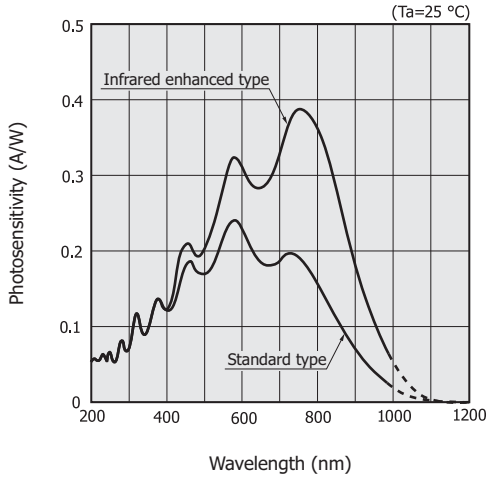
Spectral response

Figure 2-3 shows spectral response characteristics of standard type and infrared-enhanced type NMOS linear image sensors. Both types have sensitivity ranging from 200 nm to 1000 nm.

Sensitivity varies linearly with temperature. At wavelengths shorter than the peak sensitivity wavelength, however, sensitivity is stable and is not significantly dependent on temperature. The longer the wavelength region, the larger the temperature dependence, and these types exhibit a temperature coefficient of approx. 0.7%/°C at 1000 nm.

NMOS linear image sensors provide stable operation even during ultraviolet light measurement because their structure is designed to prevent sensitivity from deteriorating due to ultraviolet light.

[Figure 2-3] Spectral response (typical example)



Photoresponse nonuniformity

Image sensors contain a large number of photodiodes in arrays, and each photodiode is different from the others in terms of sensitivity. This may be due to crystalline defects in the silicon substrate or variations in processing and diffusion during the manufacturing process. In NMOS linear image sensors, these variations are evaluated in terms of photoresponse nonuniformity (PRNU) by illuminating the image sensor with uniform light emitted from a tungsten lamp and measuring variations in the output from all pixels. PRNU is given by equation (1).

$$PRNU = (\Delta X/Xave) \times 100\ [\%] \cdots\cdots\cdots (1)$$

Xave: average output of all pixels
ΔX : difference between Xave and maximum or minimum pixel output

The PRNU of our NMOS linear image sensors is specified as ±3% maximum.

Dark output

Dark output is an output that is generated even when no light strikes the image sensor. This is caused by recombination current on the photodiode surface and within the photodiode depletion layer. Although the magnitude of dark output differs from pixel to pixel, it is a fixed pattern so that the dark output component can be removed by measuring “dark state” and “light state” data and obtaining the difference between them by means of software. Dark output is temperature-dependent, so it nearly doubles for every 5 °C increase in temperature. The dark output will increase during a long exposure but can be reduced by cooling the image sensor.

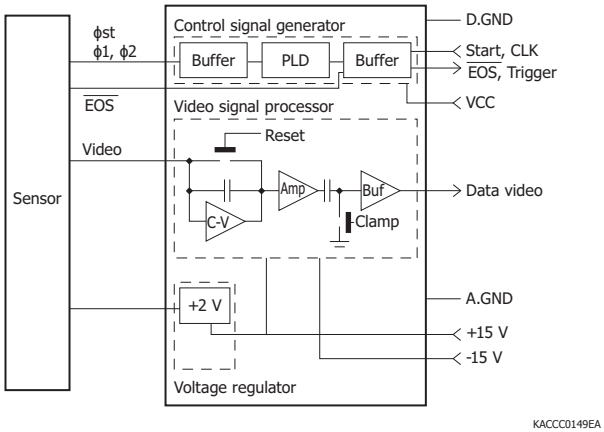
Noise and dynamic range

Noise is random output fluctuations over time and determines the detection limit in the low-light-level region. Noise includes dark current shot noise, incident light shot noise, charge amplifier reset noise, and amplifier noise. The charge amplifier reset noise can be reduced by using a clamp circuit. In NMOS linear image sensors, amplifier noise is predominant and increases as the video line capacitance becomes larger. Noise is defined by the standard deviation of the output. In the case of the S3901-128Q NMOS linear image sensor, noise is 3000 e^- rms in terms of the number of electrons and 0.5 fC rms in terms of charge. When defining the dynamic range as the ratio of the saturation charge (upper limit) to the noise (lower limit), the S3901-128Q dynamic range is 10^5 since the saturation charge is 50 pC and the noise is 0.5 fC. Effective methods for reducing the noise are to insert a low-pass filter in the signal processing circuit, perform low-speed readout, and average the data after acquiring ten or more pieces of data.

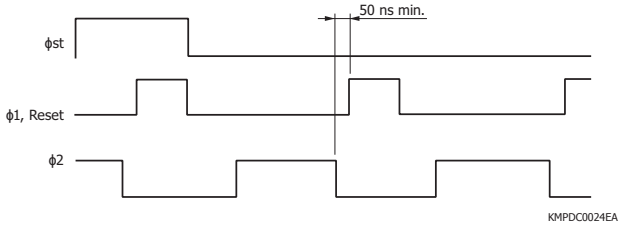
2 - 5 How to use

An external driver circuit for NMOS linear image sensors includes a digital circuit for generating input clock pulses and an analog circuit for converting output charges into voltage signals. The digital circuit consists of a clock oscillator circuit and a timing control circuit. Clock pulse signals should be input at CMOS logic levels. The analog circuit consists of an output processing circuit and an amplifier circuit. The output processing circuit normally uses a charge integration circuit including a charge amplifier. This method has the advantages that signal detection accuracy is high and it produces easy-to-process boxcar waveforms. Figure 2-4 shows a recommended block diagram of an external current integration method, and Figure 2-5 shows the timing chart.

[Figure 2-4] Recommended block diagram (external current integration method)



[Figure 2-5] Timing chart



Immediately before the address switch connected to a photodiode turns on, a reset pulse discharges the feedback capacitance in the charge amplifier. When the address switch turns on, the charge stored in the photodiode is stored in the feedback capacitor. The relationship between the output voltage (Vout) of the charge amplifier and the integrated charge (Qout) of the photodiode and the feedback capacitance (Cf) is expressed by equation (2).

$$Vout = Qout/Cf \cdots\cdots\cdots (2)$$

A capacitor of about 10 pF is used as the feedback capacitance. A clamp circuit is connected to the latter stage of the charge amplifier. The output of the clamp circuit should be connected to ground in the period immediately after the feedback capacitance is reset. This drastically reduces noise components generated when the feedback capacitance is reset.

Precautions when building driver circuits

- Separate the analog circuit ground and the digital circuit ground.
- Connect the video output terminal to the amplifier input terminal in the shortest possible distance.
- Avoid crossing of analog and digital signals as much as possible.
- Use a series power supply having only small voltage fluctuations.

3. CMOS linear image sensors

In the CMOS process, unlike NMOS process technology, digital and analog circuits can be fabricated onto the chip. CMOS linear image sensors have signal processing and timing control circuits fabricated on the image sensor chip and so need only a simple external driver circuit. Functions difficult to implement in external circuits can be built into the image sensor to make it more sophisticated. A/D converters, for example, can be fabricated on the chip to output video data as digital signals. We also welcome requests for custom devices, so feel free to consult us for special orders.

3 - 1 Features

Incorporating a signal processing circuit into the sensor chip to match the required specifications integrates the following features into the sensor. This allows downsizing the photo-sensing systems and upgrading their functions.

- High-speed response
- High gain
- Low noise
- Digital output mode (with built-in A/D converter)
- Low voltage drive (3.3 V drive)

[Table 3-1] Hamamatsu CMOS linear image sensors

Type		Type no.	Number of pixels	Pixel height (µm)	Pixel pitch (µm)	Video data rate max. (MHz)
PPS (Passive Pixel Sensor)		S9226 series*	1024	125	7.8	0.2
		S8377 series	128, 256, 512	500	50	0.5
		S8378 series	256, 512, 1024		25	
APS (Active Pixel Sensor)		S9227 series*	512	250	12.5	5
		S10453 series	512, 1024	500	25	10
	Compact	S11106-10	64	127	127	
		S11107-10	128	63.5	63.5	
	High sensitivity	S11108	2048	14	14	10
		S11639		200		
	High speed	S11105	512	250	12.5	50
Digital output		S10077	1024	50	14	1
Current output		S10121 series	128, 256, 512	2500	50	0.25
		S10124 series	256, 512, 1024		25	
		S10122 series	128, 256, 512	500	50	0.5
		S10123 series	256, 512, 1024		25	

* Surface mount type compact plastic packages are also available.

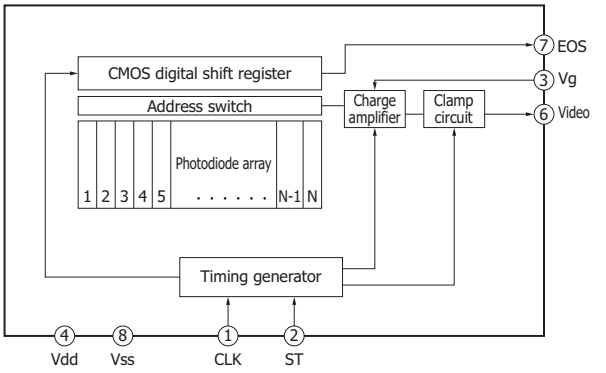
3 - 2 Operating principle and characteristics

Here we introduce the following five types among our CMOS linear image sensors.

Standard type S8377/S8378 series

The S8377/S8378 series CMOS linear image sensors have on-chip circuits that are built in an external circuit section for NMOS linear image sensors. A block diagram is shown in Figure 3-1. Like NMOS linear image sensors, these CMOS linear image sensors consist of photodiodes, address switches, and shift registers. A timing generator is formed on the input side, and a signal processing circuit made up of a charge amplifier and clamp circuit forms the readout circuit on the output side.

[Figure 3-1] Block diagram (S8377/S8378 series)



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The S8377/S8378 series operate only on a single 5 V power supply, ground, a clock pulse, and a start pulse. All pulses necessary to operate the shift register, charge amplifier, and clamp circuit are generated by the timing generator. An analog video output with boxcar waveform and an end-of-scan pulse are the output signals. The charge-to-voltage conversion gain can be adjusted in two steps by switching the charge amplifier's feedback capacitance via the input voltage to the gain selection terminal.

The peak sensitivity wavelength is 500 nm, which is shorter than NMOS linear image sensors. Since the CMOS linear image sensors operate on a single 5 V power supply, their dynamic range is narrow compared to NMOS linear image sensors that operate on ±15 V supply. However, there is almost no difference in basic characteristics such as linearity accuracy and dark output compared to NMOS linear image sensors. CMOS linear image sensors are suitable for use in compact measurement systems since they need only a simple external driver circuit.

The S8377/S8378 series are available in six types with different pixel pitches and number of pixels. A variant type, S9226-03 series, is also available having the same block configuration but a different pixel format with 7.8 µm pitch, 0.125 mm photosensitive area height, and 1024 pixels.

In the S8377/S8378 series, since the signals are read out by a single charge amplifier in the last stage, the charge amplifier must be reset each time one pixel is read out. The video data rate of the S8377/S8378 series is 500 kHz maximum.

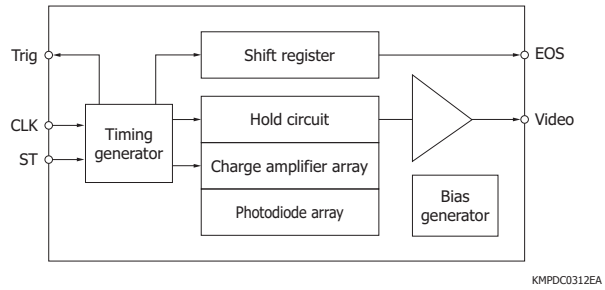
High-speed type S11105 series

The S11105 series CMOS linear image sensors have a simultaneous charge integration function for high-speed readout. Compared to the video data rate of 10 MHz maximum on the previous high-speed type (S10453 series), the S11105 series has achieved a video data rate of 50 MHz maximum. The photosensitive area consists of 512 pixels at a height of 0.25 mm, arrayed at a 12.5 µm pitch. In NMOS linear image sensors and S8377/S8378 series CMOS linear image sensors, a lag occurs in the pixel charge integration start/end times. However, the S11105 series has simultaneous integration and variable integration time functions (shutter function) controlled by an internal CMOS signal processing circuit, so charge integration in all pixels can start and end simultaneously.

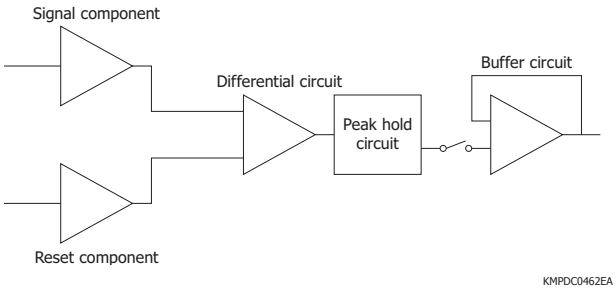
The S11105 series has a CMOS amplifier array to convert charges to voltages. The conversion gain is determined by the charge amplifier's feedback capacitance. A small feedback capacitance of 0.1 pF allows a high output voltage.

Each photodiode pixel is connected to a charge amplifier. There is no switch between the photodiode and a charge amplifier. Since the photodiodes act as a current source, the generated signal charge is not stored in the photodiodes but is stored in the charge amplifier's feedback capacitance. The output voltage from the charge amplifier changes in proportion to the incident light level during the integration time. A hold circuit is connected following the charge amplifier of each pixel. The charge amplifiers of all pixels are simultaneously reset. By inputting a hold pulse to each hold circuit immediately before the charge amplifiers are reset, the charge amplifier outputs from all pixels are simultaneously held in their respective hold circuits. The time from when the reset switch for each charge amplifier is turned off to when the hold pulse is input is the integration time. Charge integration therefore starts and ends simultaneously for all pixels. An address pulse from the shift register is next input to the switch in the stage after the hold circuit to allow the output signals being held to be sequentially output as a time-series signal from the video output terminal. Since this signal readout from the hold circuits is performed in a circuit separate from the operation for integrating the photodiode charges, the photodiodes and charge amplifiers can start the next charge integration while video output readout is in progress.

[Figure 3-2] Block diagram (S11105 series)

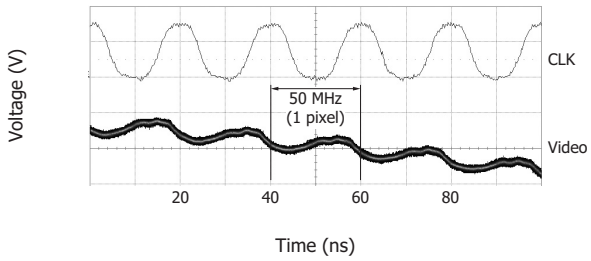


[Figure 3-3] Equivalent circuit (high-speed readout circuit of S11105 series)



The S11105 series employs a high-speed readout circuit that uses a peak-hold circuit to increase the video data rate [Figure 3-3]. The signal and reset components enter the differential circuit. Only the signal component is output and enters the peak-hold circuit, and there the output waveform is held at the peak value of the signal component. Since there is no need to reset after reading each pixel signal as in a normal circuit, signal fluctuation is reduced, making high-speed readout possible. Figure 3-4 shows the video output waveform displayed on an oscilloscope.

[Figure 3-4] Video output waveform (S11105 series)

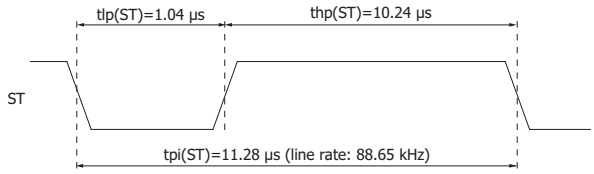


Two types of input pulses consisting of a clock pulse and a start pulse are required to operate the S11105 series. The reset pulses for the charge amplifiers, hold pulses for the hold circuits, and a start pulse for the shift register are all generated by the internal timing generator. Switching the start pulse from high to low initializes the timing generator which then sequentially generates the various control pulses. First, hold pulses are generated to hold the charge amplifier outputs in the hold circuits. Next, the reset pulses for the charge amplifiers are switched on to reset the charge amplifiers. No signal charges are integrated while the charge amplifiers are in a reset state. A start pulse is then input to the shift register to sequentially read out the video output as a time-series signal from the first pixel. When the start pulse changes from low to high, the reset pulses for the charge amplifiers are switched off, or in other words, charge integration starts. When the start pulse again changes from high to low, the timing generator is initialized as described above, and one cycle of operation is complete. Strictly speaking, charge integration starts 0.5 clocks after the start pulse has changed from low to high, and ends 0.5 clocks after the start pulse has changed from high to low. Therefore, the integration time is equal to the high period of the start pulse. If the length of one cycle is fixed, then the integration time can be adjusted by changing the ratio of high to low periods.

With the S11105 series, in addition to reading out all 512 pixels, it is possible to read out a portion of the pixels (e.g., 32 pixels from the first to the 32nd pixel) [Figure 3-6]. The line rate when reading out 512 pixels is 88.65 kHz and 595 kHz when reading out 32 pixels.

[Figure 3-6] Operation example

(a) When reading out all 512 pixels



When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (when reading out all 512 pixels).
Clock pulse frequency=Video data rate=50 MHz
Start pulse period=564/f(CLK)=564/50 MHz=11.28 µs
High start pulse period=Start pulse period - Minimum low start pulse period
=564/f(CLK) - 52/f(CLK)=564/50 MHz - 52/50 MHz=10.24 µs
The integration time corresponds to high start pulse period, which is 10.24 µs.

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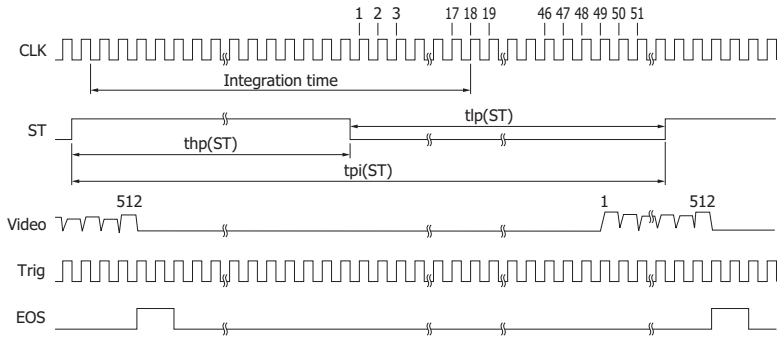
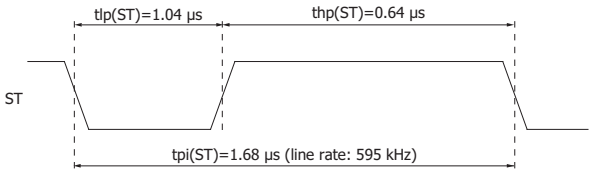
[Figure 3-5] Timing chart (S11105 series)



(b) When reading out all 1 to 32 pixels



When the clock pulse frequency is maximized (video data rate is also maximized) and the integration time is maximized (when stopping the output at channel 32).
Clock pulse frequency=Video data rate=50 MHz
Start pulse period=84/f(CLK)=84/50 MHz=1.68 µs
High start pulse period=Start pulse period - Minimum low start pulse period
=84/f(CLK) - 52/f(CLK)=84/50 MHz - 52/50 MHz=0.64 µs
The integration time corresponds to high start pulse period, which is 0.64 µs.

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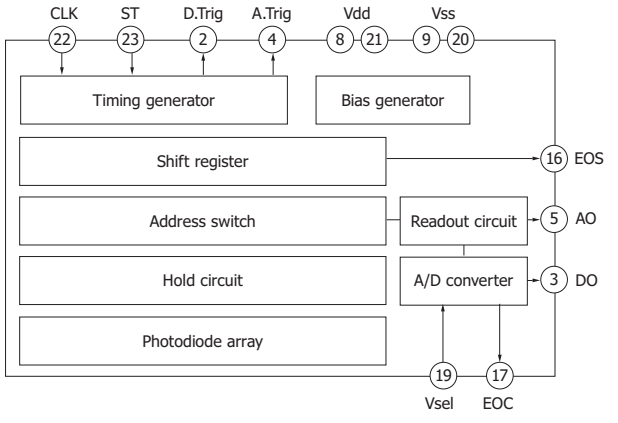
The previous S10453 series was available only in DIP packages, but the S11105 series is available in two package types: DIP (S11105) and surface mount (S11105-01).

Digital output type S10077

The S10077 is a low power consumption CMOS linear image sensor incorporating a simultaneous integration function and internal A/D converter. It provides an 8-bit or 10-bit digital output which is switchable. The video data rate is 1 MHz maximum, and the S10077 can operate from a single supply voltage of 3.3 V at a power consumption of 30 mW. The photosensitive area consists of 1024 pixels at a height of 0.05 mm, arrayed at a 14 µm pitch. The simultaneous integration and variable integration time functions (shutter function) are controlled by an internal CMOS signal processing circuit.

[Figure 3-7] Block diagram (S10077)



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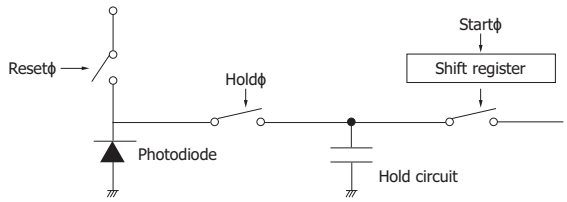
[Figure 3-8] Equivalent circuit (S10077)



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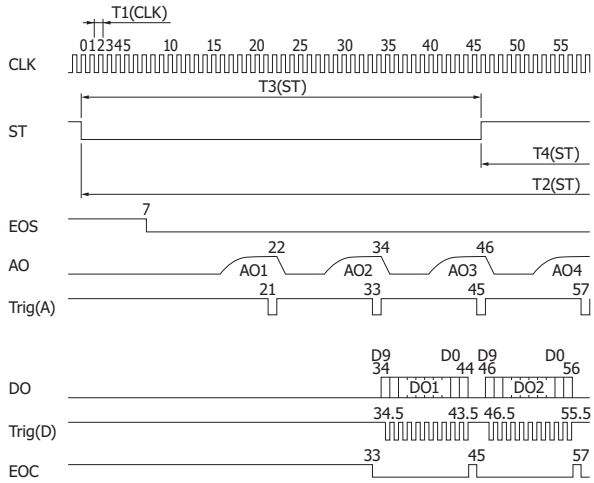
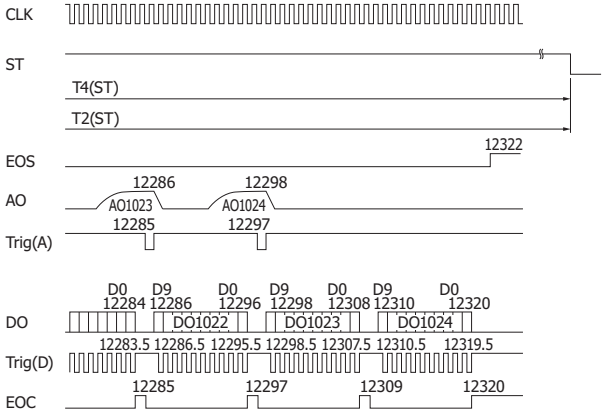
In the S10077, the signal charge stored in each photodiode is transferred to the hold circuit, and the resulting analog voltage is then sent from the readout circuit to the A/D converter via the address switch. The A/D converter converts the analog signal into a digital signal which is serially output from the MSB (most significant bit). Even though it has a small photosensitive area size, it delivers a high output voltage since the charge amplifier's feedback capacitance of the readout circuit is set to a small value of 0.05 pF. A switch and a hold circuit are connected to each photodiode pixel. During the integration time, the signal charge of each photodiode, which is proportional to the incident light level, is transferred to the hold circuit and held there. All pixels are simultaneously reset. The integration time is from when the reset switch for each photodiode is turned off to when the hold pulse is turned on and then off. An address pulse from the shift register is next input to each hold circuit to allow the output signals being held to be sequentially output as a time-series signal from the video output terminal. Since this signal readout from the hold circuits is performed in a circuit separate from the operation for integrating the photodiode charges, the photodiodes can start the next charge integration while video output readout is in progress.
Two types of input pulses consisting of a clock pulse and start pulse are required to operate the S10077 series. The reset pulses for the photodiodes, hold pulses for the hold circuits, and a start pulse for the shift register are all generated by the internal timing generator. Switching the start pulse from high to low initializes the timing generator which then sequentially generates the various control pulses. First, hold pulses are generated to hold the photodiode charges in the hold circuits. Next, the reset pulses for the photodiodes are switched on to reset the photodiodes. No signal charges are integrated while the photodiodes are in a reset state. A start pulse is then input to the shift register to sequentially read out the video output as a time-series signal from the first pixel. At the time when the start pulse changes from low to high, the reset pulses for the photodiodes are switched off, or in other words, charge integration starts. When the start pulse again changes from high to low, the timing generator is initialized as described above, and one cycle of operation is complete. Strictly speaking, charge integration starts 0.5 clocks after the start pulse has changed from low to high, and ends 7.5 clocks after the start pulse has changed from high to low. Therefore, the integration time is equal to the sum of the high period of the start pulse and the period of 7 clock pulses. Within one cycle, the integration time can be adjusted by changing the ratio of high to low periods of the start pulse.

[Figure 3-9] Timing chart (S10077, 10-bit mode)

(a) Vicinity of start pixel



(b) Vicinity of last pixel



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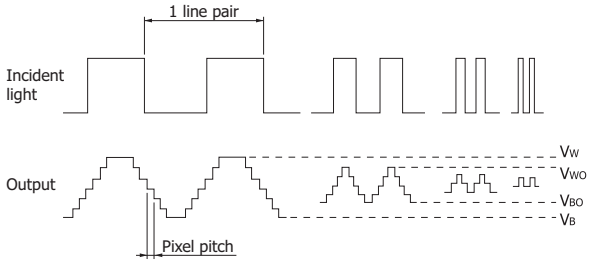
The resolution of the S10077 is indicated as a contrast transfer function. Resolution is a measure of the degree of detail to which image sensors can reproduce an input pattern. Since the photosensitive area of an image sensor consists of a number of regularly arrayed photodiodes, when an image pattern of alternating black and white lines as shown in Figure 3-10 is input, an output corresponding to the input pattern appears. As the pulse width of the input pattern becomes narrower, the difference (contrast) between the black and white level outputs becomes smaller. In such a case, the contrast transfer function (CTF) is given by equation (1).

$$CTF = \frac{V_{WO} - V_{BO}}{V_W - V_B} \quad \cdots\cdots\cdots (1)$$

V_{WO}: output white level
V_{BO} : output black level
V_W : output white level (when input pattern pulse width is wide)
V_B : output black level (when input pattern pulse width is wide)

[Figure 3-10] Contrast transfer function characteristics



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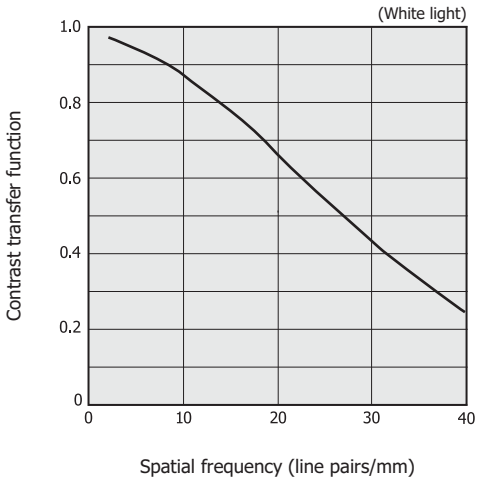
The fineness of the black and white lines for input pattern is given by the spatial frequency of the input image. The spatial frequency is the number of black and white line pairs per unit length. The higher this spatial frequency, the finer the input pattern, causing a drop in the contrast transfer function. Figure 3-11 shows an example of the S10077 contrast transfer function measurement.

[Figure 3-11] Contrast transfer function vs. spatial frequency (S10077, typical example)



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High sensitivity type S11108

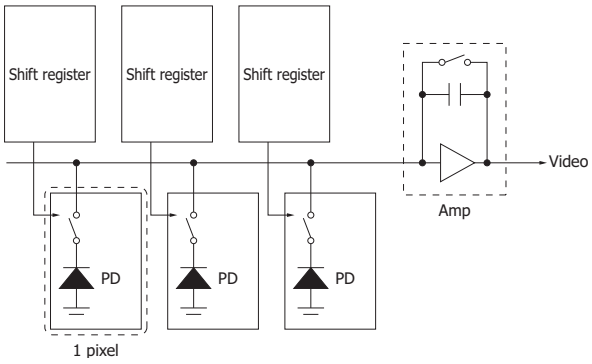
The S11108 is a 2048-pixel high sensitivity type CMOS linear image sensor with 14 × 14 µm pixel size. Its operation is easy since it only uses a 5 V supply voltage and two types of drive pulse signals.

The S11108 is designed to be used in commercial and industrial applications such as barcode readers and encoders. Compared with the previous product, it offers smaller pixel size, more pixels, and high sensitivity as well as high-speed response. In comparison with the previous PPS (passive pixel sensor) type, which performs charge-to-voltage conversion in the last-stage amplifier, the S11108 is an APS (active pixel sensor) type, which performs charge-to-voltage conversion in the amplifier available in each pixel. This achieves high sensitivity due to high efficiency. Moreover, to increase the conversion efficiency of charges generated in the photosensitive area, the charge integration capacity in the charge-to-voltage converter has been reduced. For the photosensitive area, unlike the previous surface type

photodiode structure, a buried photodiode structure was employed to reduce the dark current and shot noise in the dark state.

[Figure 3-12] Schematic (CMOS linear image sensors)

(a) PPS type



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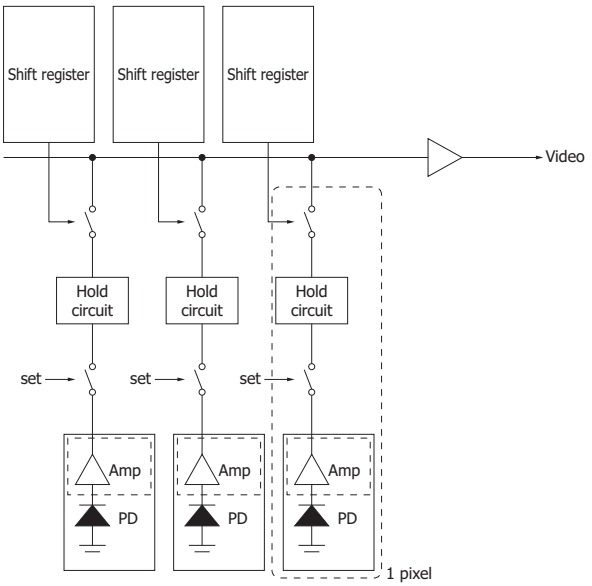
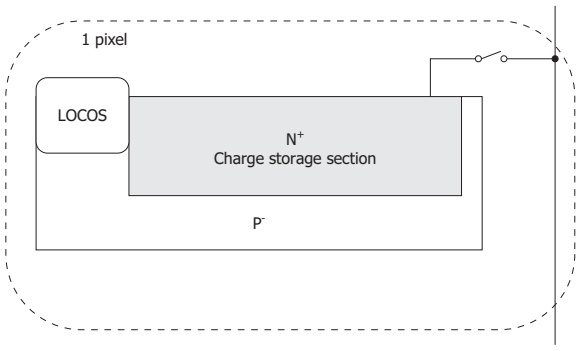
(b) APS type



KMPDC0465EA

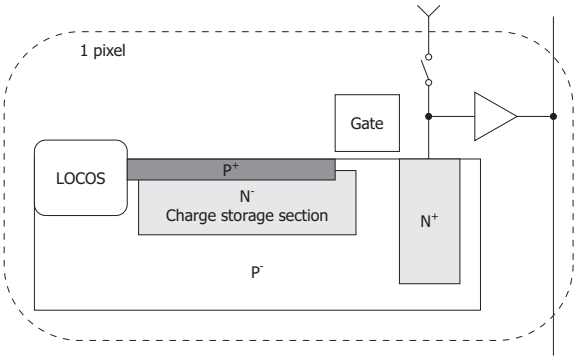
[Figure 3-13] Structure of photosensitive area

(a) Surface type photodiode



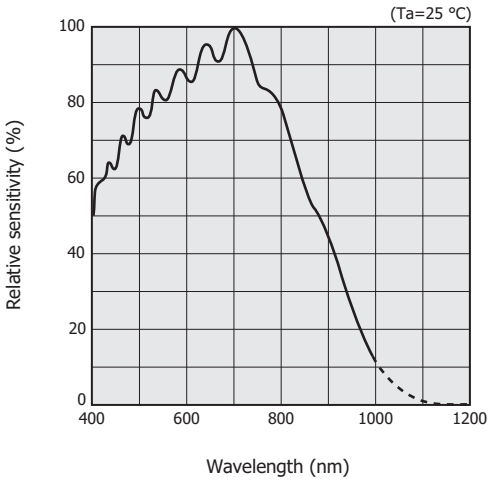
KMPDC0466EA

(b) Buried photodiode



KMPDC0467EA

[Figure 3-14] Spectral response (S11108, typical example)



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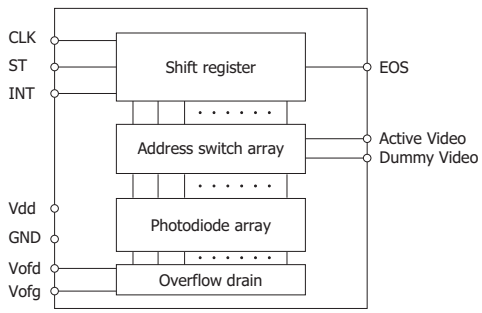
Current output type S10121 to S10124 series

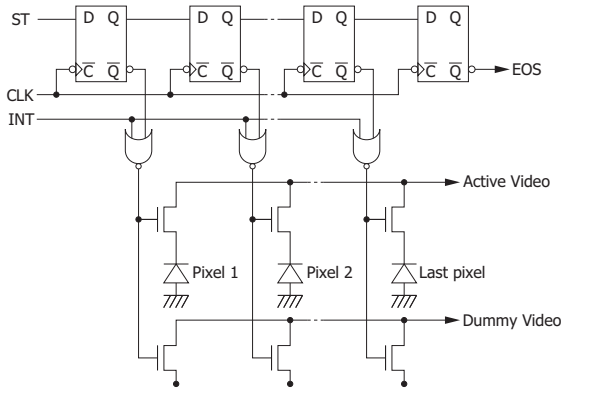
The S10121 to S10124 series are current output type CMOS linear image sensors consisting of a photodiode array that performs photoelectric conversion and stores the resulting charges, address switch array connected to each photodiode, and a shift register with a readout control function. Each address switch is a MOS switch with the source connecting to a photodiode, the gate handling the address pulses from the shift register, and the drain connecting to the video line (common output line). The shift register comprises D (delayed) type flip-flops and NOR gates.

[Figure 3-15] Block diagram (S10121 to S10124 series)



KMPDC0232EC

[Figure 3-16] Equivalent circuit (S10121 to S10124 series)



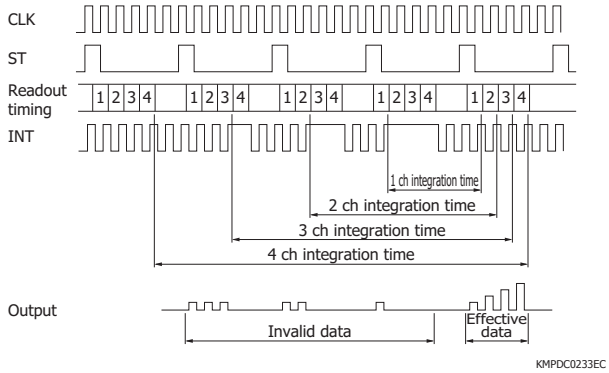
KMPDC0279EB

The structure of the S10121 to S10124 series is similar to the S3901 to S3904 series NMOS linear image sensors but different in that a shift register with readout control function is used. On the S10121 to S10124 series, the shift register output can be controlled using INT pulses. The output from the D type flip-flops and INT pulses enter the NOR gates. The output from the NOR gates is connected to the address switch gate. To perform a readout, both the output signal from the D type flip-flops and the external INT pulse must be set to low level.

The D type flip-flops start operating when a start pulse is input while a clock pulse is being applied to the D type flip-flops. The D type flip-flops synchronize to the falling edges of the clock pulses and output low level logic signals in order starting from the first pixel. Set the INT pulses for pixels that you want to read out also to low level. For pixels that you don't want to read out, set the INT pulses to high level. By controlling the INT pulses in this manner, you can selectively read out the pixels that you want. This allows the integration time to be varied for each pixel.

The timing chart of the variable integration time function is shown in Figure 3-17. Here, an example is provided for a case where the integration times of the second, third, and fourth pixels are set to twice, three times, and four times the integration time of the first pixel. The integration time can be varied for each pixel by applying INT pulses so that their durations are one cycle of the start pulse for the first pixel, two cycles for the second pixel, three cycles for the third pixel, and four cycles for the fourth pixel.

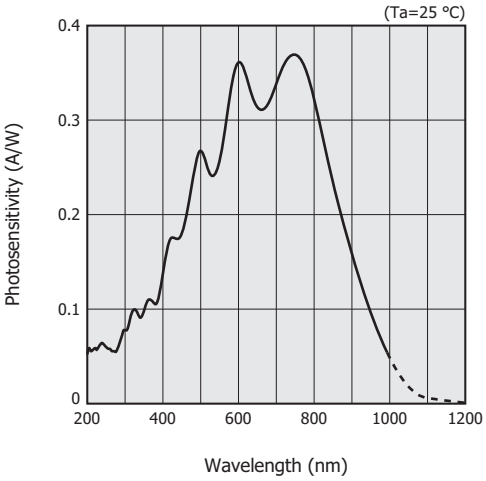
[Figure 3-17] Timing chart (variable integration time function)



KMPDC0233EC

The saturation charge of the CMOS linear image sensors is more than twice that of NMOS linear image sensors of the same pixel size [Table 3-2]. Thus, the upper limit of light level that the CMOS linear image sensors can detect is higher. Figure 3-18 shows the spectral response of the S10121 to S10124 series. The spectral response range is 200 to 1000 nm, featuring high UV sensitivity. They provide stable operation even during ultraviolet light measurement because their structure is designed to suppress sensitivity from deteriorating due to ultraviolet light.

[Figure 3-18] Spectral response
(S10121 to S10124 series, typical example)



KMPDB0399EA

[Table 3-2] Comparison table of saturation charges (NMOS linear image sensors, CMOS linear image sensors)

Product name	NMOS linear image sensor				CMOS linear image sensor			
Type no.	S3901 series	S3902 series	S3903 series	S3904 series	S10121 series	S10122 series	S10123 series	S10124 series
Pixel pitch (μm)	50		25		50		25	
Pixel height (mm)	2.5	0.5	0.5	2.5	2.5	0.5	0.5	2.5
Saturation charge (pC)	50	10	5	25	140	28	14	70

3 - 3 New approaches

Increasing the pixel size of buried photodiode structures

CMOS linear image sensors employing the buried photodiode structure have relatively small pixels with a size of 14 × 14 µm or 14 × 42 µm. Currently, we are developing larger pixel sizes such as 7 × 125 µm, 14 × 200 µm, and 127 × 127 µm. We are also in the process of incorporating additional features to the photosensitive area such as high sensitivity and high durability in the ultraviolet region and high sensitivity in the near infrared region.

Digital output

Most of the current Hamamatsu CMOS linear image sensors have analog output, but we are planning products with a 12-bit pipeline type A/D converter. This will result in an all-digital I/O interface making it easy to use and high speed.

Furthermore, we are also developing CMOS linear image sensors that integrate these endeavors.

4. CMOS area image sensors

The production of Hamamatsu CMOS area image sensors started off with sensors used in X-ray imaging such as intraoral imaging for dental diagnosis. They featured relatively large pixel sizes. In recent years, thanks to the development of buried photodiode structures, miniaturization of pixels, and improvements to readout circuits, we have been providing CMOS area image sensors that support special functions such as position and pattern detection for industrial and measurement applications, in addition to the normal imaging function.

4 - 1 Features

- High near infrared sensitivity (S11661, S11662, S12524)
- Global shutter readout (S11661, S11662, S12524)
- High-speed partial readout (S11661, S11662, S12524)
- Position detection (S9132)
- Single power supply operation
- Custom devices available (various additional functions)

4 - 2 Operating principle and characteristics

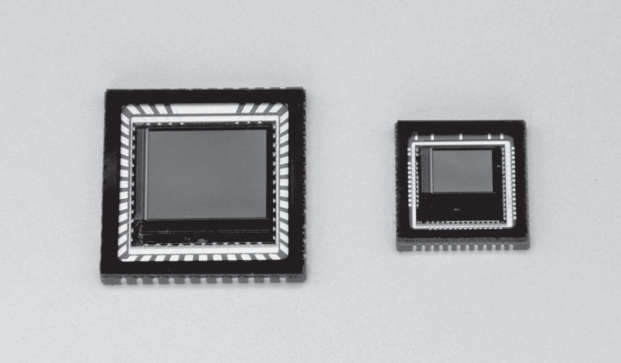
This section introduces Hamamatsu's representative CMOS area image sensors for industrial and measurement applications.

Near infrared-enhanced APS (active pixel sensor) type S11661, S11662

These CMOS area image sensors have achieved high sensitivity in the near infrared region. We offer two types: S11661, an SXGA type (1280 × 1024 pixels) and S11662, a VGA type (640 × 480 pixels). Their pixel size is 7.4 × 7.4 µm. These sensors employ a buried photodiode structure.
In a typical CMOS image sensor, four transistors are used to form a pixel, but the S11661 and S11662 use five transistors to form a pixel in order to allow global shutter readout (simultaneous integration of all pixels). To achieve wide dynamic range, voltage that exceeds 5 V is used to drive the transistors in the pixels, and the built-in charge-pump type booster circuit makes it possible to drive the image sensor using a single 3.3 V power supply. Moreover, the built-in timing circuit allows the sensor to be driven continuously with only a clock signal. The sensor is equipped with a partial readout function for reading a certain region of pixels. The reduction in the

number of pixels to be read out enables the frame rate to be increased. The partial readout region can be changed for each frame.
The S11661 and S11662 contain a pipeline type A/D converter that converts analog signals into 12-bit digital signals for output.

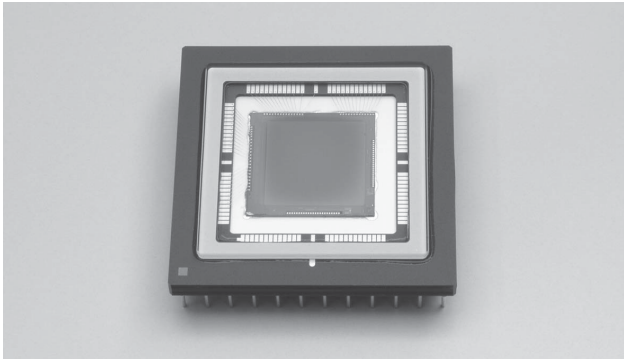
[Figure 4-1] Near infrared-enhanced APS types S11661 and S11662



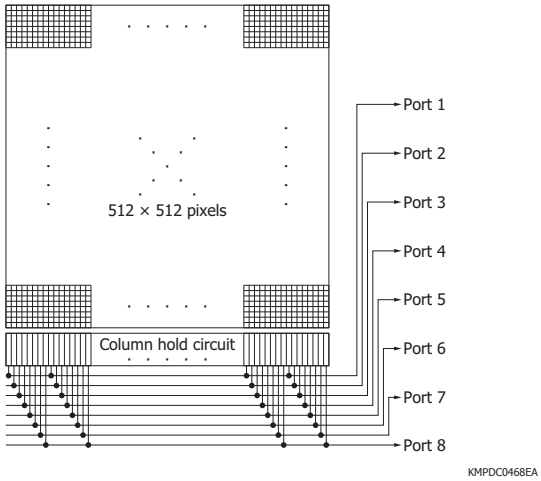
Multi-port type S12524[4)]

The S12524 is a multi-port (eight-port) CMOS area image sensor that outputs 512 × 512 pixel analog video signals in parallel. Like the S11661 and S11662, this sensor offers high sensitivity in the near infrared region. Its pixel size is 20 × 20 µm. It employs a buried photodiode structure. To make global shutter readout possible, each pixel is made up of five transistors. The built-in timing circuit consists of the minimal necessary circuitry, and both the vertical scanning circuit and horizontal scanning circuit can be directly controlled externally. External control makes it possible to specify where and how many regions to be read out, and a moving object can be tracked by changing the partial readout region for each frame.
A block diagram is shown in Figure 4-3. The sensor is contrived to keep the readout load of the eight ports uniform even during partial readout. During a full-screen readout of 512 × 512 pixels, imaging is possible at 250 frames/s maximum. During a partial readout of four regions of 64 × 64 pixels, imaging is possible at 880 frames/s maximum. Note that the S12524 is used in the high-speed sensor head of Hamamatsu intelligent vision sensor [Figure 4-4].

[Figure 4-2] Multi-port type S12524



[Figure 4-3] Block diagram (S12524)



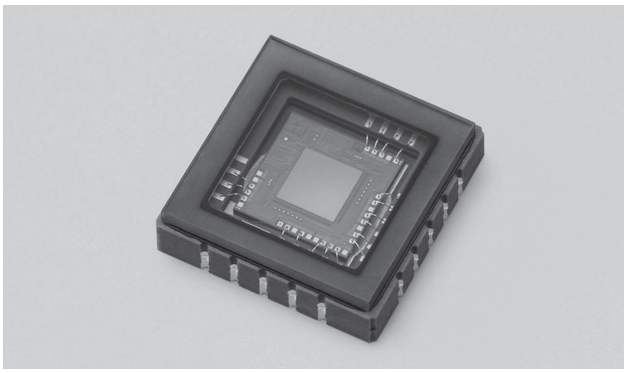
[Figure 4-4] High-speed sensor head of intelligent vision sensor

Profile sensor S9132[5)]

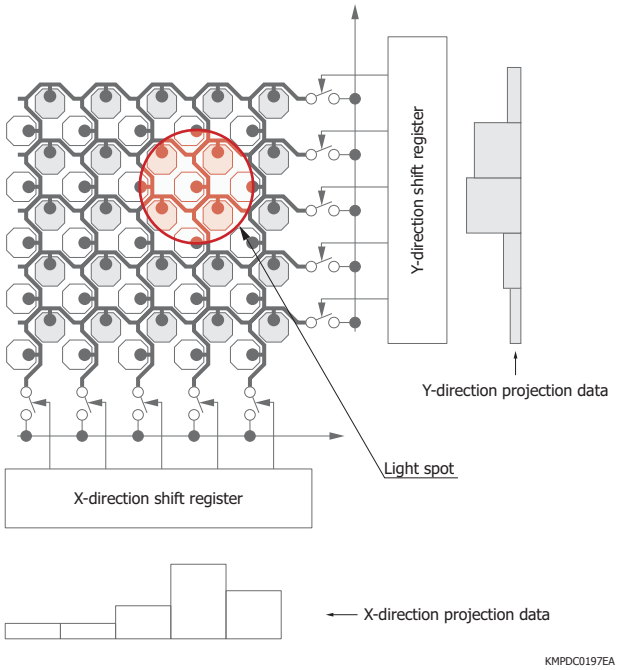
The profile sensor is a CMOS area image sensor designed specifically for acquiring projection profile data. Projection profile data contains a full set of data of a line of output; position information and luminance information of the input light spot can be acquired from this data. The photosensitive area of the profile sensor is divided into a photosensitive area for the X direction and that for the Y direction [Figure 4-6]. For the photosensitive area for the X direction, the photosensitive area of one column is connected with metal wiring. And, for the photosensitive area for the Y direction, the photosensitive area of one row is connected with metal wiring. This allows the projection profile data of the X-axis and Y-axis to be read out. A readout amplifier and A/D converter are provided for each direction, X and Y, allowing each direction to be controlled separately.
Since the data size of the projection profile data for the X and Y directions of the profile sensor is small, position detection and moving object detection of light spots can be performed faster than normal area image sensors. The pixel rate is 833 kHz. When 256 pixels are read out, the frame rate is 3200 frames/s maximum. Typically, a two-dimensional PSD is used for light spot detection. However, the profile sensor is advantageous in that it improves output linearity, it can detect multiple light spots, and it simplifies the external driver circuit.

Since the sensor chip contains a timing generator, bias voltage generator circuit, and successive approximation type 10-bit A/D converter, it can be operated with an extremely simple external driver circuit and external signal processing circuit.

[Figure 4-5] Profile sensor S9132



[Figure 4-6] Operating principle (profile sensor)



4 - 3 New approaches

Column parallel ADC type

If we categorize image sensors by the number of A/D converters, we have a type that has a single high-speed A/D converter on a chip, and another type that has a low-speed A/D converter for each column (column parallel type ADC). With advances in CMOS micromachining technology, there is a growing number of cases where image sensors with column parallel type ADC are used in high-speed low-noise applications. The performance advantages of column parallel type ADCs become apparent especially when the image sensor has large number of pixels.

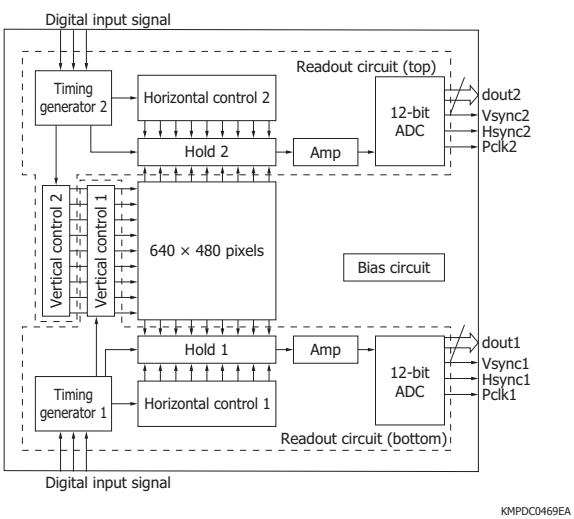
Hamamatsu has mainly been producing CMOS area image sensors with a single A/D converter on a chip, but in recent years, we have been developing various types of column parallel type ADCs. We are also developing readout circuits for monolithic, high-speed, low-noise CMOS area image sensors as well as hybrid image sensors that combines a CCD and compound semiconductor (e.g., InGaAs).

2-port parallel output type

Hamamatsu is developing CMOS area image sensors with a variety of built-in functions. As an example, a 2-port parallel output type is described below. The 2-port parallel output type has a readout circuit on the top and bottom of the photosensitive area as shown in Figure 4-7, and each circuit can be operated independently. A video line for each circuit is connected to each pixel, and the data of any pixel can be read out from either circuit. This circuit structure allows, for example, the top half of the photosensitive area to be read using the top circuit and the bottom half of the photosensitive area to be read using the bottom circuit. As another example, one circuit could read out a specific small region at a high frame rate, and the other circuit could read out the remaining regions at a normal frame rate. When this sensor is used as an optical communication image sensor that performs optical communication and imaging in parallel, numerous readout modes shown below can be used.

① Normal imaging mode (640 × 480 pixels, 40 frames/s, the remaining port is paused)
② Double-speed imaging mode (top half of 640 × 240 pixels: 80 frames/s, bottom half: 80 frames/s)
③ Blinking light source detection mode (odd lines of 640 × 240 pixels: 80 frames/s, even lines: 80 frames/s)
④ Imaging and communication (1 location) parallel mode (640 × 479 pixels: 40 frames/s, 32 × 1 pixels: 100 kHz)
⑤ Imaging and communication (3 location) parallel mode (640 × 477 pixels: 40 frames/s, 136 × 1 pixels × 3 regions: 20 kHz)
⑥ Communication (2 location) parallel mode (32 × 1 pixels: 100 kHz, 32 × 1 pixels: 100 kHz)

[Figure 4-7] Block diagram (2-port parallel output type)



5. Distance image sensors

Distance image sensors are image sensors that measure the distance to the target object using the TOF (time-of-flight) method. Used in combination with a pulse modulated light source, these image sensors output phase (time) difference information of emitted and received light. Distance data can be obtained by performing calculation on the output signal with an external signal processing circuit or on a PC.

5 - 1 Features

- High-speed charge transfer
- Wide dynamic range and low noise by non-destructive readout (S11961/S11963-01CR)
- Built-in column gain amplifier (S11963-01CR)
  Gain: × 1, × 2, × 4
- Fewer detection errors even under fluctuating background light (charge drain function)
- Real-time distance measurement

5 - 2 Structure

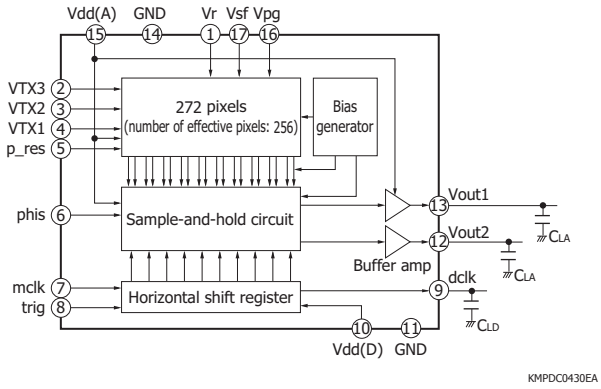
Distance image sensors consist of a photosensitive area, shift register, output buffer amplifier, bias generator, timing generator, and so on. The block diagram is shown in Figure 5-1. Distance image sensors are different from typical CMOS image sensors in the following manner.

· Pixel structure that allows high-speed charge transfer
· Outputs two phase signals representing distance information from two output terminals

Like a typical CMOS image sensor, the output signal from the photosensitive area is processed by the sample-and-hold circuit or column gain amplifier circuit, scanned sequentially by the shift register, and read out as voltage output.

[Figure 5-1] Block diagram

(a) S11961-01CR



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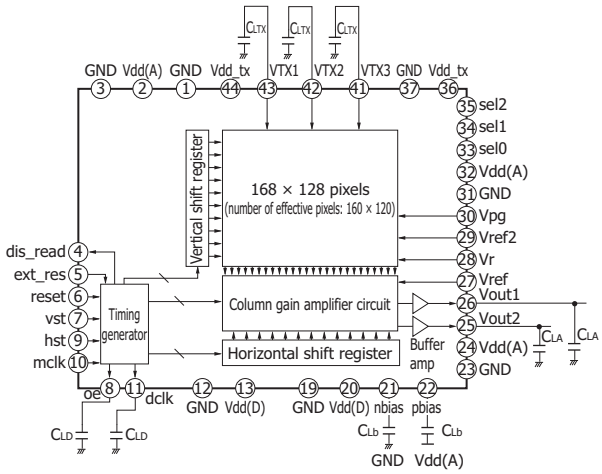
(b) S11963-01CR



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5 - 3 Operating principle

The timing chart of the photosensitive area of the distance image sensor is shown in Figure 5-2. Output voltages V_1 and V_2 obtained by applying charge-to-voltage conversion on accumulated charges Q_1 and Q_2 based on their integration capacitances Cfd_1 and Cfd_2 are expressed by equations (1) and (2).

$$V_1 = Q_1/Cfd_1 = N \times Iph \times \{(T_0 - Td)/Cfd_1\} \cdots\cdots (1)$$

$$V_2 = Q_2/Cfd_2 = N \times Iph \times (Td/Cfd_2) \cdots\cdots\cdots\cdots (2)$$

Cfd_1, Cfd_2: integration capacitance of each output
N : charge transfer clock count
Iph : photocurrent
T_0 : pulse width
Td : delay time

[Table 5-1] Hamamatsu distance image sensors

Type no.	Type	Number of pixels	Pixel size [μm (H) × μm (V)]	Package	Dimensions (mm)
S11961-01CR	Linear image sensor	256	20 × 50	Surface mount type PWB	10.6 × 5.8 × 2.0
S11962-01CR	Area image sensor	64 × 64	40 × 40		8.18 × 9.26 × 2.0
S11963-01CR		160 × 120	30 × 30		11.85 × 9.5 × 2.0

Delay time Td when Cfd_1=Cfd_2 in equations (1) and (2) is expressed by equation (3).

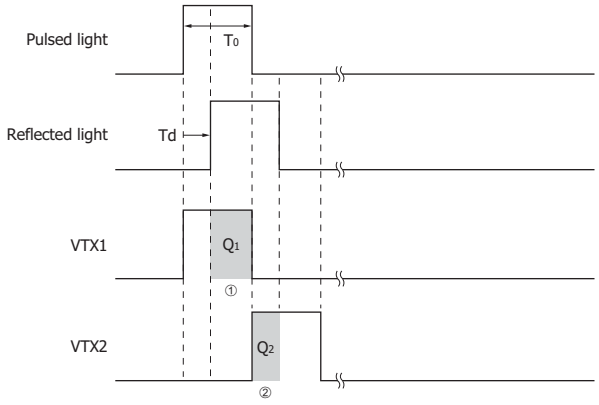
$$Td = \{V_2/(V_1 + V_2)\} \times T_0 \cdots\cdots (3)$$

Using the values (V_1, V_2) output according to the distance, distance (L) is expressed by equation (4).

$$L = 1/2 \times c \times Td = 1/2 \times c \times \{V_2/(V_1 + V_2)\} \times T_0 \cdots\cdots\cdots (4)$$

c: speed of light (3×10^8 m/s)

[Figure 5-2] Timing chart of photosensitive area



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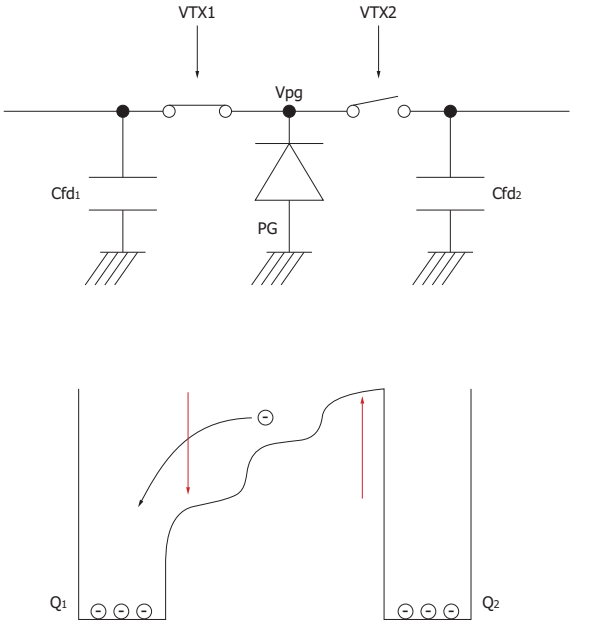
The structure and surface potential of the photosensitive area of the distance image sensor are shown in Figure 5-3. Typical CMOS image sensors can be driven with a single power supply, but the transfer time needed for the charge to move from the photosensitive area to the integration area is in the microsecond order. On the other hand, high-speed charge transfer (nanosecond order) is possible on CCD image sensors, but they require multiple voltage inputs including high voltage.

To achieve the high-speed charge transfer (several tens of nanoseconds) needed to acquire distance information, we have developed a pixel structure that enables high-speed charge transfer like the CCDs in the CMOS process. This has allowed distance image sensors to achieve the high-speed charge transfer needed for distance measurement.

The number of electrons generated in each pulse emission is several e^-. Therefore, the operation shown in Figure 5-3 is repeated several thousand to several tens of thousands of times, and then the accumulated charge is read out. The number of repetitions varies depending on the incident light level and the required accuracy of distance measurement.

[Figure 5-3] Structure and surface potential of photosensitive area

(a) VTX1: on, VTX2: off (in the case of Figure 5-2 ①)



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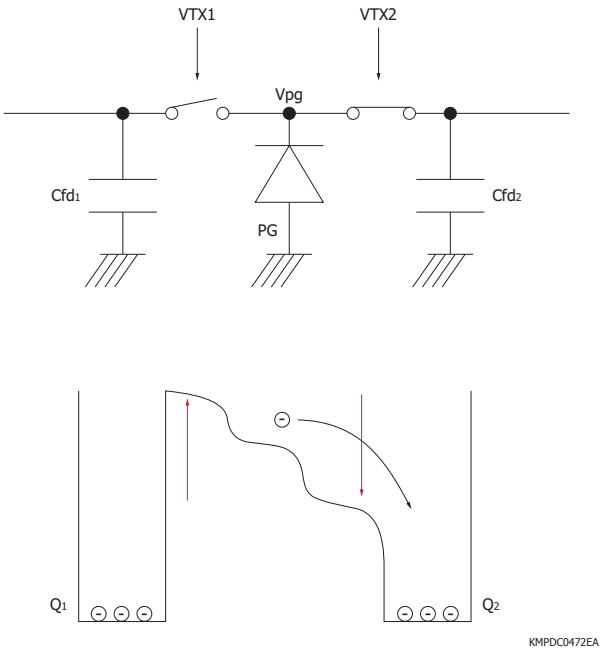
(b) VTX1: off, VTX2: on (in the case of Figure 5-2 ②)



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[Table 5-2] Distance measurement range and VTX1, VTX2, and light-emission pulse widths

Distance measurement range max. (m)	VTX1, VTX2, light-emission pulse widths (ns)
4.5	30
6	40
9	60

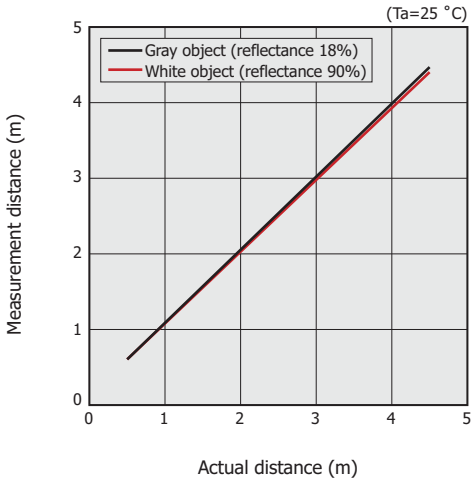
Note: Light travels approximately 30 cm in 1 ns.

5 - 4 Characteristics

Figures 5-4 and 5-5 show distance measurement examples under the following conditions using the S11961-01CR and a light source.

· Integration time=30 ms (effective integration time=180 µs)
· Charge transfer clock width (VTX1, VTX2)=30 ns
· Light receiving lens F=1.2, angle of view=37.5° × 27.7°
· Light source output=10 W, duty ratio=0.3%,
light emission pulse width=30 ns, λ=870 nm
· Light projection angle=10° × 10°
· Background light: room light level

[Figure 5-4] Measurement distance vs. actual distance (S11961-01CR, center pixel of photosensitive area, typical example)



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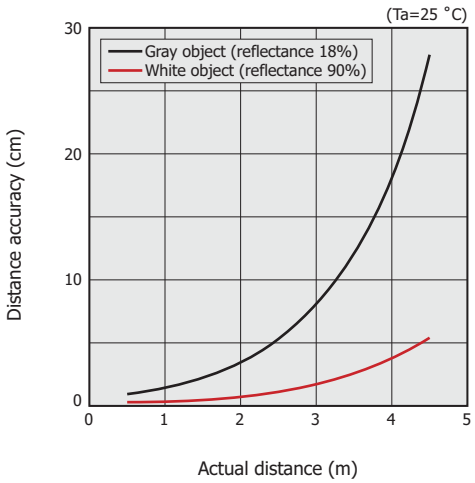
[Figure 5-5] Distance accuracy vs. actual distance (S11961-01CR, the center pixel of the photosensitive area, typical example)



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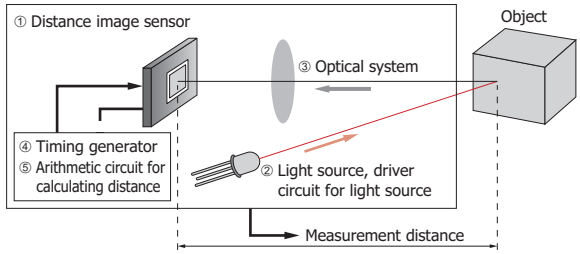
5 - 5 How to use

To operate the distance image sensor, supply voltages, timing signals, and bias voltages must be applied. For the S11963-01CR, two types of supply voltages are required: Vdd at 5 V and Vdd_tx at 3 V. In addition, timing signals (ext_res, reset, vst, hst, mclk, VTX1, VTX2, and VTX3) needs to be generated with an external circuit and applied (see the datasheet). Note that because VTX1, VTX2, and VTX3 are high-speed clock pulse signals, high-speed buffer ICs must be provided near the distance image sensor. Bias voltages (Vr, Vpg, Vref, and Vref2) must be applied within the ranges specified in the datasheet.

Configuration example

A configuration example of a distance measurement system using the distance image sensor is shown in Figure 5-6. The system consists of the distance image sensor, light source and its driver circuit, light emitting/receiving optical system, timing generator, and arithmetic circuit for calculating distance. The distance accuracy depends greatly on the light source emission level and the light emitting/receiving optical system.

[Figure 5-6] Configuration example of distance measurement system



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Light source selection

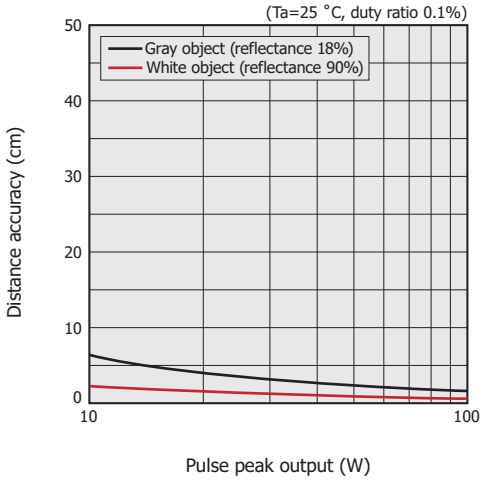
When the distance image sensor is used to measure distance, a light source (LED or pulse laser diode) suitable for the pulse width of the distance image sensor's charge transfer clock must be selected. For example, to measure up to 4.5 m, the pulse width of the charge transfer clock and the light emission pulse width must be set to 30 ns. Thus, the response speed of the light source needs to be around 10 ns or less for rise and fall times. Since the light source must be irradiated in a line in the case of the S11961-01CR distance linear image sensor and over an area in the case of the S11962-01CR and S11963-01CR distance area image sensors, large output power is required. For this, multiple light sources are sometimes used. When multiple light sources are used, a driver circuit for driving the multiple light sources at high speeds and high output is also required. An estimation example expressing the relationship between the light source pulse peak output and the distance accuracy is shown in Figure 5-7.

◉ Conditions

· Integration time=16 ms (effective integration time=32 µs)
· Charge transfer clock width (VTX1, VTX2)=30 ns
· Light receiving lens F=1.2, focal distance f=2.8 mm
· Light emission pulse width=30 ns, λ=870 nm
· Light projection angle=20° × 20°
· Background light: room light level

[Figure 5-7] Distance accuracy vs. pulse peak output (estimation example)

(a) Measurement distance: 1 m



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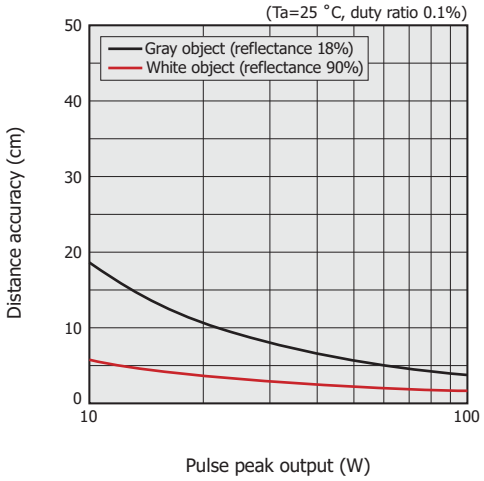
(b) Measurement distance: 2 m



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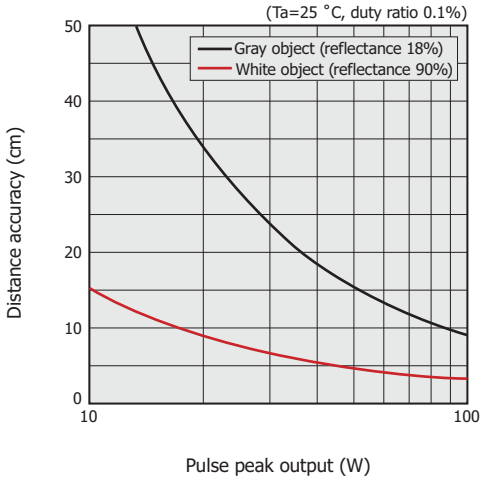
(c) Measurement distance: 4 m



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6. Photodiode arrays with amplifiers

Photodiodes with amplifiers are a type of CMOS linear image sensor designed for long and narrow area detection systems using an equal-magnification optical system. These devices combine a Si photodiode array with a CMOS signal processing IC. The CMOS signal processing IC contains a timing generator, shift register, hold circuit, and charge amplifier array, so only a simple external circuit is needed. A long and narrow image sensor can be configured by arranging multiple devices in a row. For X-ray detection applications, we also offer photodiode array/amplifier devices with a phosphor screen attached directly to their photosensitive area.

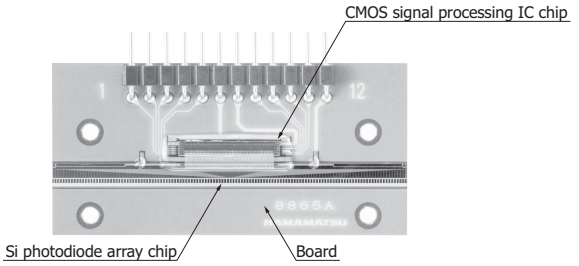
6 - 1 Features

- Long and narrow sensor can be configured by placement of multiple devices.
- 5 V operation
- Simultaneous integration by charge amplifier
- Time-series signal readout by shift register (data rate: 1 MHz max.)
- Low dark current due to zero-bias photodiode operation
- Internal clamp circuit achieves low noise and wide dynamic range.
- Internal timing generator allows operation with two types of input pulses (reset and clock).
- X-ray detection type available with a phosphor screen attached to the photosensitive area
- Usable with wide variety of photodiode specifications (custom order product)

6 - 2 Structure

As shown in Figure 6-1, a photodiode array with amplifier consists of two chips: a Si photodiode array chip for light detection and a CMOS signal processing IC chip.

[Figure 6-1] Structure diagram (S11865 series)



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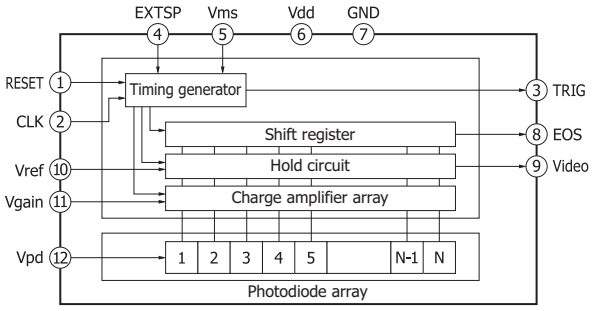
Signals from 64 pixels or 128 pixels at a time are handled by the CMOS signal processing IC. This makes the entire system configuration very simple compared to methods that connect each pixel on the photodiode array to an external signal processing circuit.

Sensor devices with a phosphor screen attached to the photosensitive area are intended for X-ray detection. When X-rays irradiate a sensor device, the phosphor screen converts the X-rays into visible light which is then detected by the photodiode array. These devices are used as line sensors for X-ray non-destructive inspection tasks requiring long X-ray detectors.

6 - 3 Operating principle

The CMOS signal processing IC chip consists of a timing generator, shift register, hold circuit, and charge amplifier array [Figure 6-2]. Each pixel of the photodiode array is connected by wire bonding to the charge amplifier in the CMOS signal processing IC chip. The light-generated charge (Qout) in a photodiode, which is expressed by the product of the photocurrent (I_L) and the integration time (Ts), is converted into an output voltage (Vout = Qout/Cf) by the charge amplifier feedback capacitance (Cf). The output signal, which is sent to the hold circuit before the charge amplifier is reset, is read out by the shift register as time-series voltage signals. In the S11865/S11866 series, signals from all pixels are read out by the simultaneous integration method. The S11865/S11866 series also have a shutter function capable of adjusting the integration time. The video data rate is 1 MHz maximum.

[Figure 6-2] Block diagram (S11865-64/-128, S11866-64-02/-128-02)



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[Table 6-1] Hamamatsu photodiode arrays with amplifiers

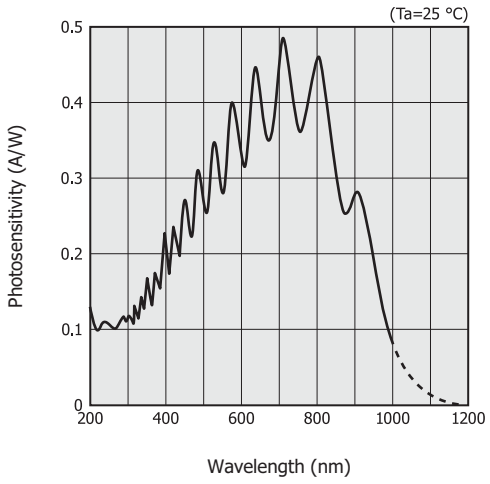
Type no.	Pixel height (mm)	Pixel pitch (mm)	Number of pixels	Line rate (lines/s)
S11865-64	0.8	0.8	64	14678
S11865-128	0.6	0.4	128	7568
S11865-256	0.3	0.2	256	3844
S11866-64-02	1.6	1.6	64	14678
S11866-128-02	0.8	0.8	128	7568

Note: We also offer X-ray detection types with a phosphor screen attached directly to their photosensitive area.

6 - 4 Characteristics

Figure 6-3 shows the spectral response of the S11865/S11866 series.

[Figure 6-3] Spectral response (S11865/S11866 series, typical example)



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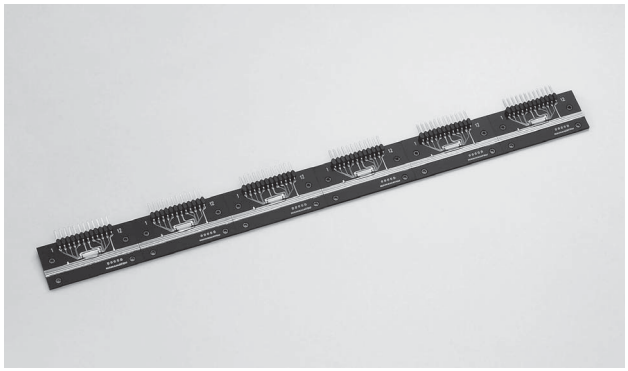
6 - 5 How to use

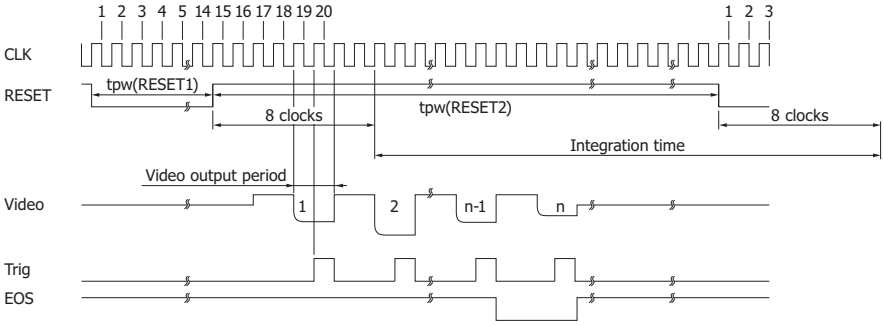
The S11865/S11866 series are designed so that the effective area length equals the board length. This allows easily configuring a long and narrow, one-dimensional detector system by arranging multiple sensors in a row. This type of system is difficult to create with normal image sensors. When multiple sensors are arrayed, the output signal from each sensor can be read out in parallel using multiple external circuits or read out serially using a single circuit. To read out signals serially, set the external voltage so that the preceding-stage end-of-scan signal is used as the next-stage start signal.

Besides fabricating image sensors with a long detection length, photodiode arrays with amplifiers also allow downsizing of detection systems. Using our standard CMOS signal processing IC chips makes it easy to create custom image sensors by just changing the Si photodiode array chips or circuit boards to a desired shape.

[Figure 6-5] Long and narrow image sensor consisting of multiple photodiode arrays with amplifiers



[Figure 6-4] Timing chart (S11865/S11866 series)



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7. InGaAs linear image sensors

InGaAs linear image sensors are designed specifically for near infrared detection. These image sensors successfully minimize adverse effects from dark current by driving the InGaAs photodiode array at zero bias, and they deliver a wide dynamic range in the near infrared region.

7 - 1 Features

- Wide dynamic range
- Low dark current due to zero bias operation
- Wide spectral response range
- High gain due to charge amplifier
- Low noise due to CDS circuit
- Internal saturation control circuit
- Internal timing generator allows simple operation.
- Low crosstalk
- Selectable gain
- Hybrid type: includes a back-illuminated chip for different spectral response ranges

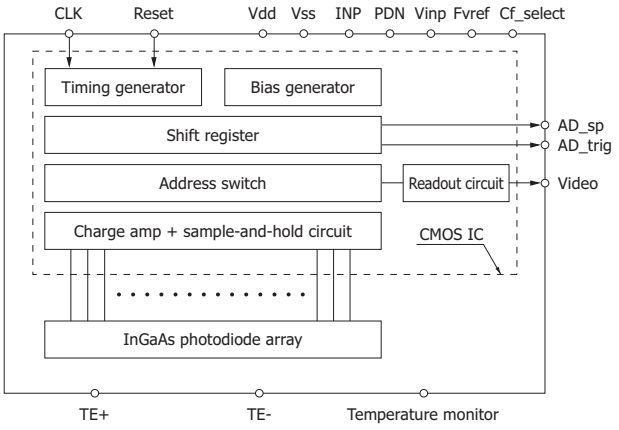
7 - 2 Structure

InGaAs linear image sensors consist of an InGaAs photodiode array and a CMOS IC (ROIC) including a charge amplifier array, sample-and-hold circuit, shift register, readout circuit, and timing generator. The InGaAs photodiode array is connected to the CMOS IC by wire bonding or via bumps. Available packages include a ceramic package for room temperature operation and a metal package with a built-in thermoelectric cooler, which are selectable according to application. A typical block diagram for TE-cooled InGaAs linear image sensors is shown in Figure 7-1. An analog video output (Video) and digital outputs (AD_trig, AD_sp) for sample-and-hold can be obtained by supplying analog inputs of +5 V (Vdd), GND (Vss), a charge amplifier reset voltage (INP), pixel voltage (PDN), and readout circuit reset voltages (Vinp, Vref, Fvref), as well as digital inputs of master clock pulse (CLK) and integration time control pulse (Reset).

[Table 7-1] Hamamatsu InGaAs linear image sensors

Illumination type	Type	Spectral response range (μm)	Number of pixels	Pixel size [μm (H) × μm (V)]	Package
Front-illuminated type	Standard type	0.9 to 1.7	128	50 × 250	Ceramic
			256	50 × 250, 50 × 500	Ceramic, Metal
			512	25 × 250, 25 × 500	
	High-speed type		256	50 × 50	Ceramic
			512	25 × 25	
			1024	25 × 25, 25 × 100	
	Long wavelength type	0.9 to 1.85	256	50 × 250	Metal
			512	25 × 250	
		0.9 to 2.05	256	50 × 250	
		0.9 to 2.15	256	50 × 250	
			512	25 × 250	
		0.9 to 2.25	256	50 × 250	
		0.9 to 2.55	256	50 × 250	
			512	25 × 250	
Back-illuminated type	Standard type	0.95 to 1.7	256	50 × 50, 50 × 500	Ceramic, Metal
			512	25 × 25, 25 × 500	
	Hybrid type	0.95 to 2.15	512 (256 + 256)	25 × 250	Metal

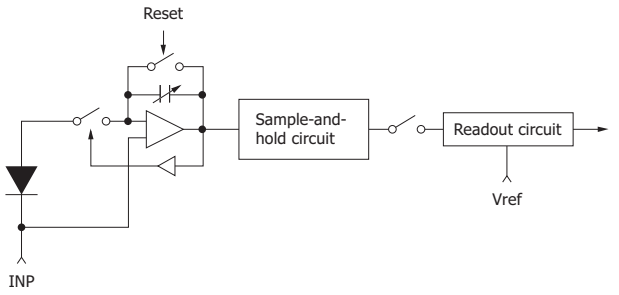
[Figure 7-1] Block diagram (TE-cooled type)



7 - 3 Operating principle

In the CMOS IC for InGaAs linear image sensors, a "charge amplifier and sample-and-hold circuit" array is formed and connected one-to-one to each pixel on the InGaAs photodiode array. Figure 7-2 shows an equivalent circuit for one pixel.

[Figure 7-2] Equivalent circuit (for one pixel)



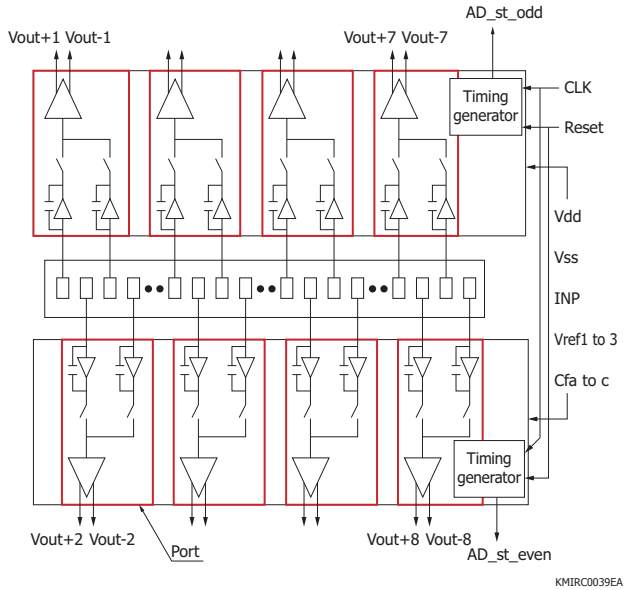
When light enters the photodiodes of an InGaAs linear image sensor, electric charges are generated and flow into the feedback capacitance of the charge amplifier. This differential-input charge amplifier can operate photodiodes at nearly zero bias, which suppresses the dark current. In actual operation, however, the amplifier has an offset voltage and the supply voltage to each pixel varies by several millivolts, so the video output of some pixels goes positive versus the reset level, while that of other pixels goes negative. Therefore, when no light is incident on the image sensor, extending the integration time increases the output on both the positive and negative sides. However, this output caused by the dark current is a fixed pattern, so only the output signal resulting from light input can be extracted by subtracting the output due to the dark current from the output signal obtained with light incident on the image sensor. Since InGaAs photodiodes are made from a compound semiconductor, there are lattice defects and the dark current has relatively large absolute values and variations compared to Si photodiodes. The maximum integration time (integration time needed to reach saturation due to dark current) of InGaAs photodiodes therefore varies among the pixels. If a pixel with high dark current becomes saturated yet the charge integration still continues, then the charges that are no longer stored in the charge amplifier's feedback capacitance will flow out to the adjacent pixels, degrading the purity of the signal output (this is known as "blooming"). To avoid this blooming, each pixel has a circuit for stopping the charge integration by sensing whether the charge amplifier's feedback capacitance is saturated.

To extract continuous signals, the integration capacitance of the charge amplifier must be reset. A drawback of this, however, is that a large reset noise occurs. This reset noise must be removed to make measurements with high accuracy. In the CDS circuit for InGaAs linear image sensors, the integration start output is held in the signal processing circuit immediately after reset and the integration end output is then held to obtain the difference between the two outputs to eliminate the reset switching noise.

Incidentally, high-speed type image sensor circuitry gives priority to high-speed readout while standard type image sensor circuitry gives priority to a wide dynamic range.

To achieve even higher speeds, the multi-port types employ a multiport readout format that reads out the data in parallel by dividing the pixels into multiple ports.

[Figure 7-3] Multi-port example (8-port)



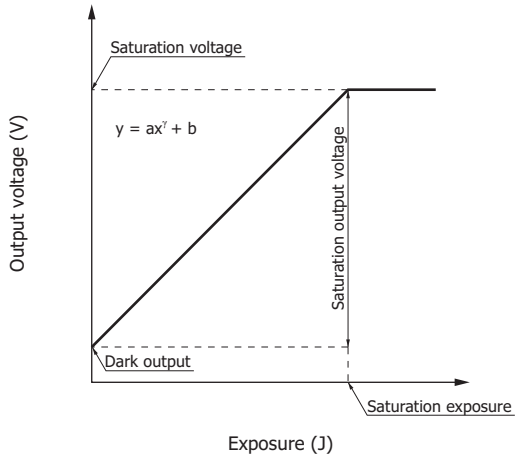
7 - 4 Characteristics

Input/output characteristics

The relation between the light level incident to the image sensor and the signal output is referred to as the input/output characteristics. Since InGaAs linear image sensors operate in charge amplifier mode, the incident light exposure (unit: J) is expressed by the product of light level (unit: W) and integration time (unit: s).

The output from an InGaAs linear image sensor is represented in voltage. Figure 7-4 shows a schematic graph of input/output characteristics. The slope in the figure can be expressed by equation (1).

[Figure 7-4] Schematic graph of input/output characteristics (log graph)



$$y = ax^{\gamma} + b \quad \cdots\cdots\cdots\cdots (1)$$

y: output voltage
a: sensitivity (ratio of output with respect to exposure)
x: exposure
γ: slope coefficient
b: dark output (output when exposure=0)

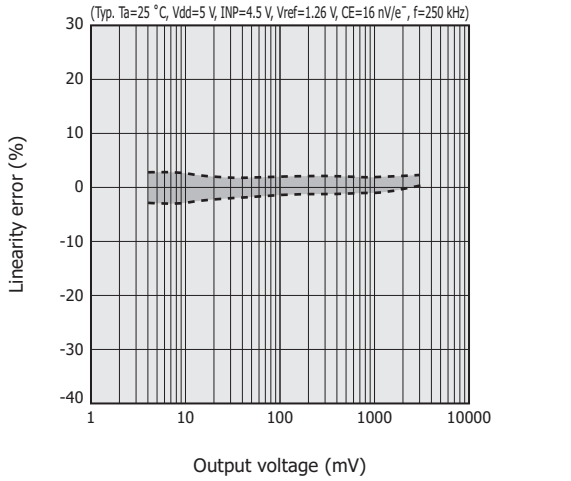
Since the upper limit of the output voltage is determined by the output voltage range of the charge amplifier, the input/output characteristics will have an inflection point even if the incident light exposure is increased linearly. The incident light exposure at this inflection point is referred to as the saturation exposure, the output voltage as the saturation output voltage, and the amount of charge stored in the charge amplifier as the saturation charge.
In our InGaAs linear image sensor datasheets, the saturation output voltage (Vsat) is defined as the saturated output voltage from light input minus the dark output. Under the condition that no light is incident on the sensor (dark state), extending the integration time causes the output to increase on the positive and negative sides. The voltage going negative becomes saturated at approx. 0.5 V.
The saturation charge is calculated from the equation Q = C V based on the saturation output voltage. If the integration capacitance (Cf) is 10 pF and the saturation output voltage is 3.2 V, then the saturation charge will be 32 pC.

Linearity error

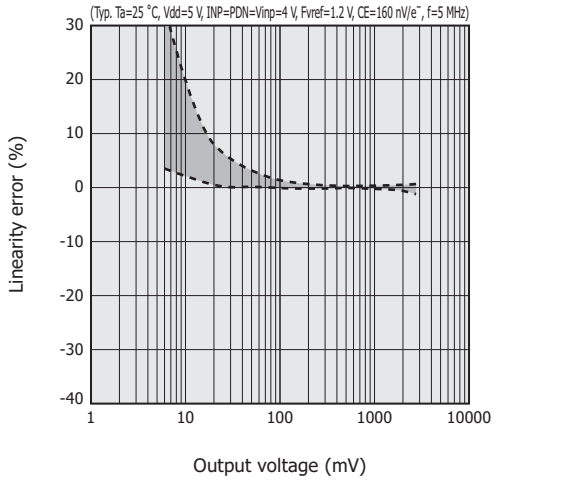
The slope coefficient (γ) of input/output characteristics shown in the preceding section corresponds to the slope plotted on the logarithmic graph. This γ value is 1, but during actual measurement, the input/output characteristics will slightly deviate from this. This deviation is known as the linearity error and is expressed in percentage.
Figure 7-5 shows the linearity error obtained by random sampling. The linearity error of the G9204-512S at 95% or below the saturation exposure is within ±3%, which is quite small. The G12230-512WB is an improved type designed to reduce the linearity error at high gain (CE=160 nV/e⁻).

[Figure 7-5] Linearity error

(a) G9204-512S



(b) G12230-512WB (λc=1.7 µm chip)



Spectral response

When light energy incident on the photosensitive area formed with a PN junction is greater than the InGaAs band gap energy, the electrons in the valence band are excited into the conduction band, generating electron/hole pairs. This generated charge diffuses toward the photodiode depletion layer where the electric field accelerates the charge to pass through the PN junction, resulting in a signal for readout. If the light energy is smaller than the band gap energy, it cannot be detected. The cutoff wavelength (λc) is given by equation (2).

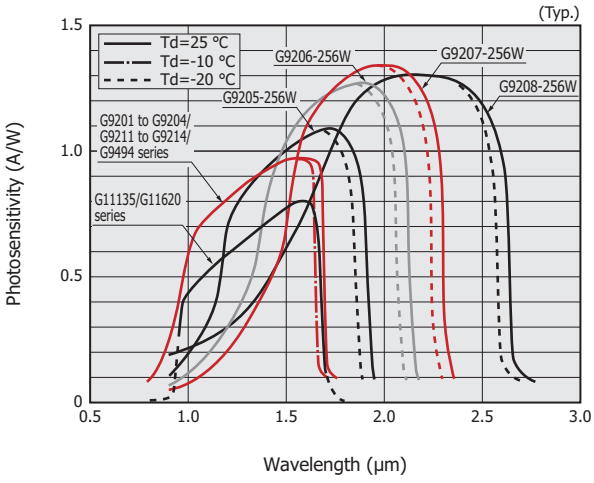
$$\lambda c = \frac{1.24}{Eg} \ [\mu m] \quad \cdots\cdots\cdots\cdots (2)$$

Eg: band gap energy [eV]

The band gap energy for $InxGa_{1-x}As$ (x=0.53) is 0.73 eV at room temperature, so the cutoff wavelength will be 1.7 µm. On the long wavelength type $InxGa_{1-x}As$ (x=0.82), the band gap energy is 0.48 eV at room temperatures, so the cutoff wavelength will be 2.6 µm.

The light absorption coefficient for InGaAs differs depending on the light wavelength. The longer the light wavelength, the smaller the light absorption coefficient, and near the cutoff wavelength it decreases abruptly. The incident light at longer wavelengths penetrates deeper into the InGaAs substrate, generating carriers in deep positions within it. Since these carriers have a limited life, they can only diffuse a certain distance (diffusion length) after being generated. This means that, even when the same amount of light enters the InGaAs linear image sensor, the probability that the generated carriers can reach the depletion layer and eventually be detected as an output signal depends on the wavelength. Moreover, how the incident light undergoes interference, reflection, and absorption on the surface passivation film of the photodiode (such as the insulation film) depends on the wavelength and affects the sensitivity.
Figures 7-6 and 7-7 show examples of spectral response. The spectral response varies with the temperature. This is because the band gap energy is temperature-dependent. The InGaAs band gap energy increases as the temperature drops, causing the peak sensitivity wavelength and cutoff wavelength to shift to the short wavelength side.

[Figure 7-6] Spectral response



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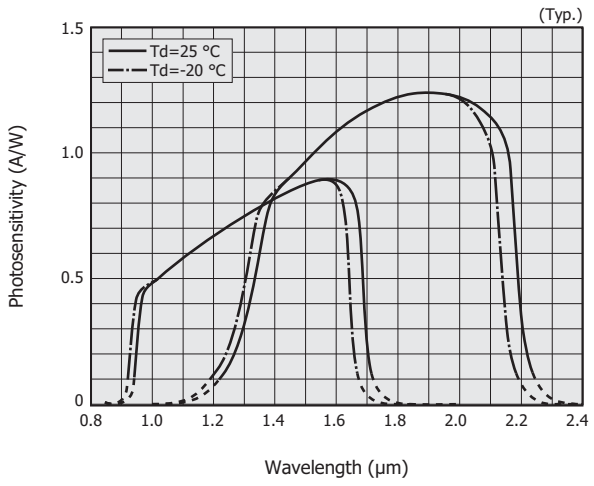
[Figure 7-7] Spectral response (G12230-512WB)



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Photoresponse nonuniformity

InGaAs linear image sensors contain a large number of InGaAs photodiodes arranged in an array, yet sensitivity of each photodiode (pixel) is not uniform. This may result from crystal defects in the InGaAs substrate and/or variations in the processing and diffusion in the manufacturing process as well as inconsistencies in the CMOS charge amplifier arrays. For our InGaAs linear image sensors, variations in the outputs from all pixels measured when the effective photosensitive area of each photodiode is uniformly illuminated are referred to as photoresponse nonuniformity (PRNU) and defined as shown in equation (3).

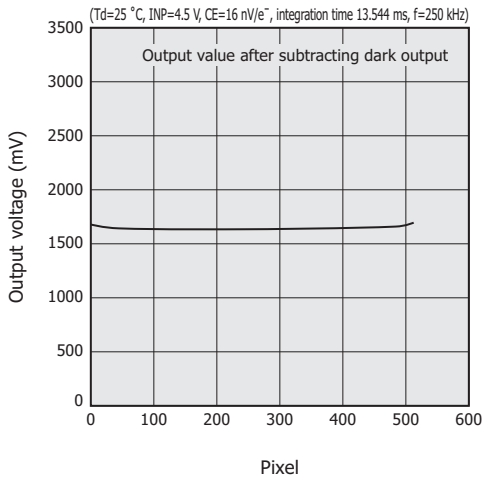
$$PRNU = (\Delta X/X) \times 100\ [\%] \cdots\cdots\cdots (3)$$

X : average output of all pixels
ΔX: absolute value of the difference between the average output X and the output of the maximum (or minimum) output pixel

In our outgoing product inspection for photoresponse nonuniformity, the output is adjusted to approx. 50% of the saturation output voltage and a halogen lamp is used as the light source. Since InGaAs linear image sensors use a compound semiconductor crystal for light detection, the photodiode array may contain crystal defects, resulting in abnormal output signals from some of the pixels (defect pixels). The photoresponse nonuniformity specification is ±5% to ±20%.
Scratches and dust on the light input window may also cause the sensitivity uniformity to deteriorate. So caution should be exercised on this point when handling image sensors. Figure 7-8 shows typical examples of photoresponse nonuniformity. These data were obtained by random sampling.

[Figure 7-8] Photoresponse nonuniformity (typical example)

(a) G9204-512S



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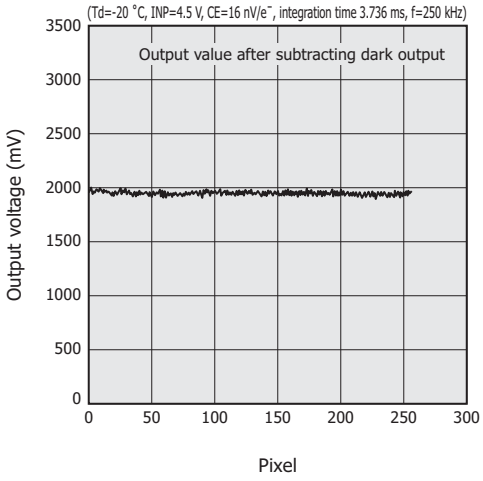
(b) G9207-256W



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Dark output

The dark output is the output generated even when no incident light is present. This output is caused by the dark current (sum of diffusion current, recombination current, and surface leakage current) of the photodiode, which flows to charge the charge amplifier and is converted into a voltage output. Since the upper limit of the output is determined by the saturation output voltage, a large dark output narrows the dynamic range of the output signal. The output signal is the sum of the output generated by light and the dark output, so the purity of the output signal can be improved by using signal processing to subtract the dark output from each pixel.

The dark output is given by equation (4). The integration time must be determined by taking the magnitude of the dark output into account.

$$Vd = I_D \times (Ts/Cf) + Voff \quad \cdots\cdots\cdots\cdots (4)$$

Vd : dark output [V]
I_D : dark current [pA]
Ts : integration time [s]
Cf : integration capacitance [pF]
Voff: ROIC offset voltage [V]

When rewriting the above equation in terms of integration time (Ts) by substituting the saturation output voltage (Vsat) for the dark output (Vd), the maximum integration time (Tsmax) is expressed by equation (5).

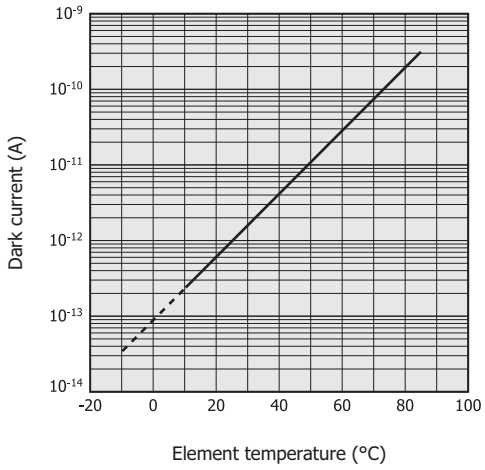
$$Tsmax = Cf \times Vsat/I_D \quad \cdots\cdots\cdots\cdots (5)$$

The band gap widens as the temperature decreases, so the number of carriers thermally excited into the valence band from the conduction band decreases, causing the dark current to reduce exponentially with the temperature. In our InGaAs linear image sensors, the temperature coefficient β of the dark current is 1.06 to 1.1. If the dark current at temperature T_1 (unit: °C) is I_{DT1} (unit: A), then the dark current I_{DT} at temperature T is given by equation (6).

$$I_{DT} = I_{DT1} \times \beta^{(T - T_1)} \text{ [A]} \quad \cdots\cdots\cdots\cdots (6)$$

Figure 7-9 shows the temperature characteristics of the G9204- 512S dark current (random sampling).

[Figure 7-9] Dark current vs. element temperature (G9204-512S, typical example)



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Noise

InGaAs linear image sensor noise can be largely divided into fixed pattern noise and random noise.

Fixed pattern noise includes photodiode dark current which is current noise from the DC component. The magnitude of the fixed pattern noise is constant even if readout conditions are changed, so it can be canceled by using an external signal processing circuit.

Random noise, on the other hand, results from fluctuations in voltage, current, or charge that are caused in the signal output process in the sensor. When the fixed pattern noise has been canceled by external signal processing, the random noise will then determine the InGaAs linear image sensor's lower detection limit or lower limit of dynamic range.

Random noise includes the following four components:

① Dark current shot noise (Nd)
② Signal current shot noise at light input (Ns)
③ Charge amplifier reset noise (Nr)
④ CMOS charge amplifier readout noise (N_R)

In general, the reset noise ③ that occurs when the charge amplifier is reset is predominant. This reset noise can be greatly reduced with a CDS circuit, so the dark current shot noise ① and CMOS charge amplifier readout noise ④ become significant sources of noise. Dark current shot noise results from erratic generation of the output charge due to dark current. This noise becomes larger as the output charge due to dark current increases, and therefore varies depending on operating conditions such as integration time and temperature.

Signal current shot noise ② is caused by fluctuations due to incident photons arriving randomly at the sensor.

The total noise (N) is expressed by equation (7).

$$N = \sqrt{Nd^2 + Ns^2 + N_R^2} \quad \cdots\cdots\cdots\cdots (7)$$

The dark current shot noise (Nd) and signal current shot noise at light input (Ns) can be expressed as the root square of the generated charge by representing them as an "equivalent input noise charge" which is a value converted to a charge quantity for input to the image sensor.

$$Nd = \sqrt{\frac{2I_D}{q}} \times Ts \ [e^- \text{ rms}] \quad \cdots\cdots\cdots\cdots (8)$$

$$Ns = \sqrt{\frac{2I_S}{q}} \times Ts \ [e^- \text{ rms}] \quad \cdots\cdots\cdots\cdots (9)$$

Is: signal current by light input
q : electron charge

We specify the noise level in InGaAs linear image sensors as fluctuations in the output voltage of each pixel by using root-mean-square noise voltage (V rms) units. Converting equations (8) and (9) into voltage therefore gives equations (10) and (11), respectively.

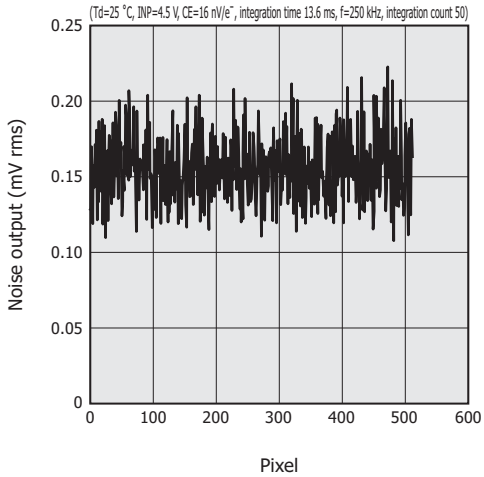
$$Nd = \sqrt{2q\ I_D} \times \frac{Ts}{Cf} \ [\text{V rms}] \quad \cdots\cdots\cdots\cdots (10)$$

$$Ns = \sqrt{2q\ I_S} \times \frac{Ts}{Cf} \ [\text{V rms}] \quad \cdots\cdots\cdots\cdots (11)$$

When the CMOS charge amplifier readout noise (N_R) is measured at 25 °C using an integration time of 1 ms, a data rate of 250 kHz, and an integration count of 50, the standard deviation in the G9201 series is calculated to be 180 µV rms at Cf=10 pF and 400 µV rms at Cf=0.5 pF. The noise levels listed for the G9201/G9211 series in our datasheet are measured at 25 °C using an integration time of 10 to 20 ms, data rate of 250 kHz, and integration count of 50 in order to calculate the standard deviation. In the G9205 to G9208 series, this measurement is made at -20 °C using an integration time of 1 ms or less, data rate of 250 kHz, and integration count of 50. Figure 7-10 shows output noise fluctuations measured with the G9204-512S and G9207-256W with no incident light. These data were obtained by random sampling.

[Figure 7-10] Noise output fluctuations (typical example)

(a) G9204-512S



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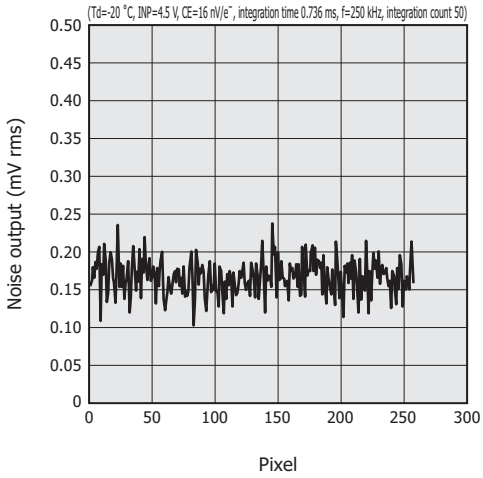
(b) G9207-256W



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7 - 5 How to use

This section explains how to use and operate InGaAs linear image sensors including handling precautions and setting operating conditions.

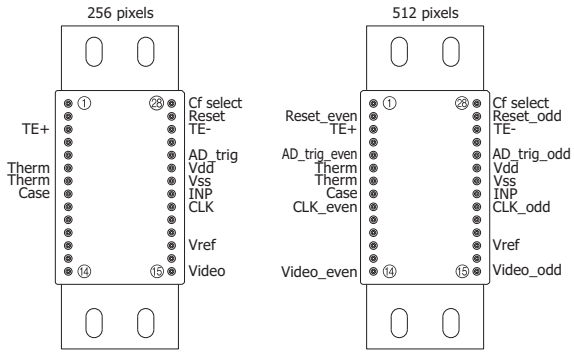
Setups

There are two types of InGaAs linear image sensors: a thermoelectrically cooled type that contains a thermoelectric cooler and thermistor, and a non-cooled type. Both types basically operate with the same drive method except for cooling operation.

(1) Terminal description

Make connections by referring to Figures 7-11 and 7-12 and to Table 7-2.

[Figure 7-11] Pin connections (G9201 to G9204 series, top view)



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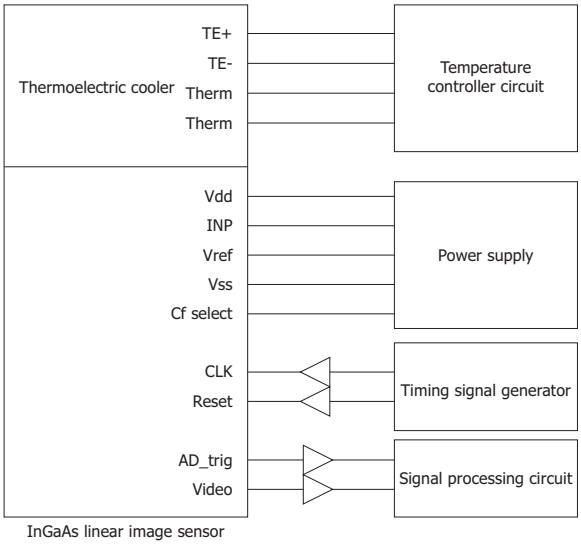
[Figure 7-12] Setup and wiring (G9201 to G9204 series)



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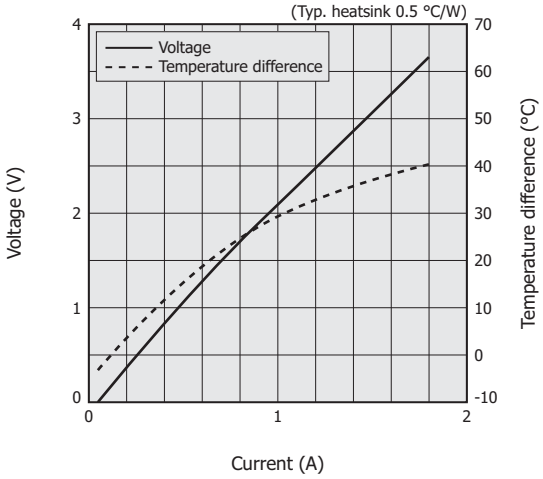
(2) Heatsink

• Selecting a heatsink

When cooling a one-stage thermoelectrically cooled device to -10 °C, select a heatsink of 0.5 °C/W or less including a safety margin. When cooling a two-stage thermoelectrically cooled device to -20 °C, select a heatsink of 0.4 °C/W or less. Equipment should be carefully designed so that the heatsink is not placed where heat builds up. Provide good air ventilation to allow heat emitted from the heatsink to sufficiently dissipate by installing air fans and ventilation ducts. Note that the heatsink thermal resistance varies according to forced air cooling.

[Figure 7-13] Temperature characteristics of one-stage thermoelectrically cooled device



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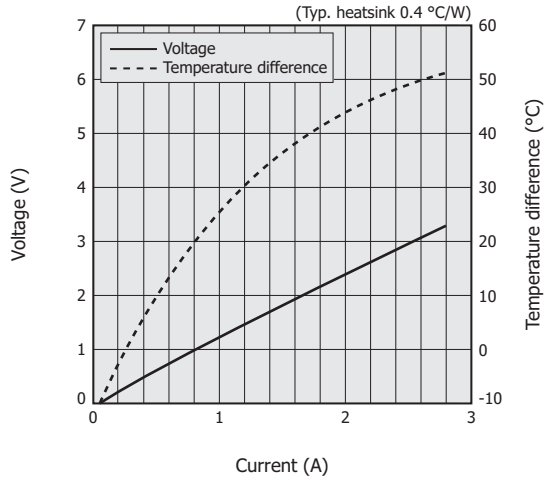
[Figure 7-14] Temperature characteristics of two-stage thermoelectrically cooled device



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[Table 7-2] Terminal function and recommended connection (G9201 to G9204 series)

Terminal name	Input/output	Function and recommended connection
CLK	Input (CMOS logic)	Clock pulse for operating the CMOS shift register
Reset	Input (CMOS logic)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is the integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip
Vss	–	Ground for the signal processing circuit on the CMOS chip
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip
Cf select	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip
Case	–	This terminal is connected to the package.
Therm	–	Thermistor terminal for monitoring temperature inside the package
TE+, TE-	–	Power supply terminal for the thermoelectric cooler for cooling the photodiode array
AD_trig	Output	Digital signal for A/D conversion; positive polarity
Video	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit on the CMOS chip

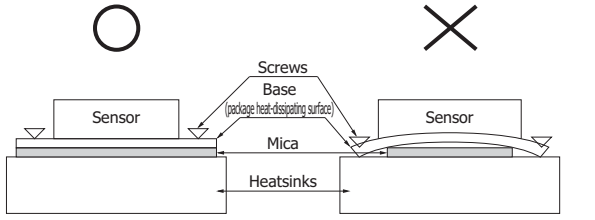
• Heatsink mounting method

To allow the thermoelectric cooler to exhibit fullest cooling capacity, the heatsink must be mounted correctly onto the sensor package. Mount the heatsink while taking the following precautions.

- Check that the heatsink attachment surface and the heat-dissipating surface of the InGaAs image sensor package are clean and flat.
- Mount the heatsink so that it makes tight contact with the entire heat-dissipating surface of the package. The heat-dissipating surface area should be large to improve the cooling efficiency and prevent possible damage.
- Apply a thin coat of heat-conductive grease uniformly over the attachment surface in order to lower thermal resistance between the package heat-dissipating surface and the heatsink. Fasten the sensor package to the heatsink with screws using equal force so that the grease spreads more uniformly. When a mica sheet is used, it must also make contact with the entire heat-dissipating surface of the package. The cooling efficiency will degrade if the sensor package is fastened to the heatsink with screws while the mica sheet is still too small to cover the screw positions. This may also warp the package base, causing cracks between the sensor and the package base [Figure 7-15 (a)].
- Do not press on the upper side of the package when fastening the sensor package to the heatsink or printed circuit board. If stress is applied to the glass faceplate, this may cause the faceplate to come off or may impair airtightness of the package [Figure 7-15 (b)].

[Figure 7-15] Sensor mounting method

(a) Example 1



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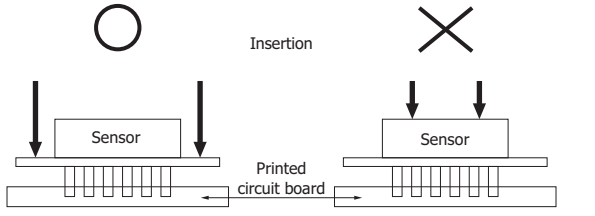
(b) Example 2



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(3) Video signal monitoring

The image sensor output end does not have drive capability, so in order to monitor the video signal, the sensor output should be amplified by a buffer amplifier and then fed to an oscilloscope.

Drive method

Sensor operation should be checked in a dark state. Block the light falling on the photosensitive area before checking operation.

(1) Turning on power to the driver circuit

First check the voltages (Vdd, INP, Vref, etc.) supplied to the sensor, and then turn the power on. At this point, also check that the current values are correct. If excessive current is flowing, the power supply line might be shorted so immediately turn off the power and check the power supply line.

(2) Inputting control signals from the pulse generator

While referring to the timing chart shown in Figure 7-16, input the control signals from the pulse generator to the InGaAs linear image sensor (G9201/G11135 series). Two control signals (CLK and Reset) are input to the image sensor and must be H-CMOS level inputs. The image sensor may malfunction if other control signal levels are used. In the G9201/G9494 series, set the Reset signal pulse width to at least 6 µs. The CLK signal frequency determines the video signal readout frequency, and the Reset pulse interval determines the integration time.
Normal operation is performed whether the CLK and Reset signals are synchronized or not. When the Reset pulse rising edge is synchronized with the CLK pulse falling edge, the integration starts at the falling edge of the CLK pulse following the Reset pulse rising edge. When not synchronized, the integration starts at the falling edge of the second CLK pulse from the Reset pulse rising edge. When the Reset pulse falling edge is synchronized with the CLK pulse falling edge, the integration ends with the falling edge of the CLK pulse following the Reset pulse falling edge. If not synchronized, the integration ends with the falling edge of the second CLK pulse from the Reset pulse falling edge.

(3) Setting the drive timing

• Example 1: When operating an InGaAs linear image sensor G9201-256S at CLK frequency of 1 MHz

Since the video signal readout frequency is 1/8 of the CLK signal frequency, the readout time (tr) per pixel is 8 µs. The time required for one scan (tscan) is therefore given by equation (12).

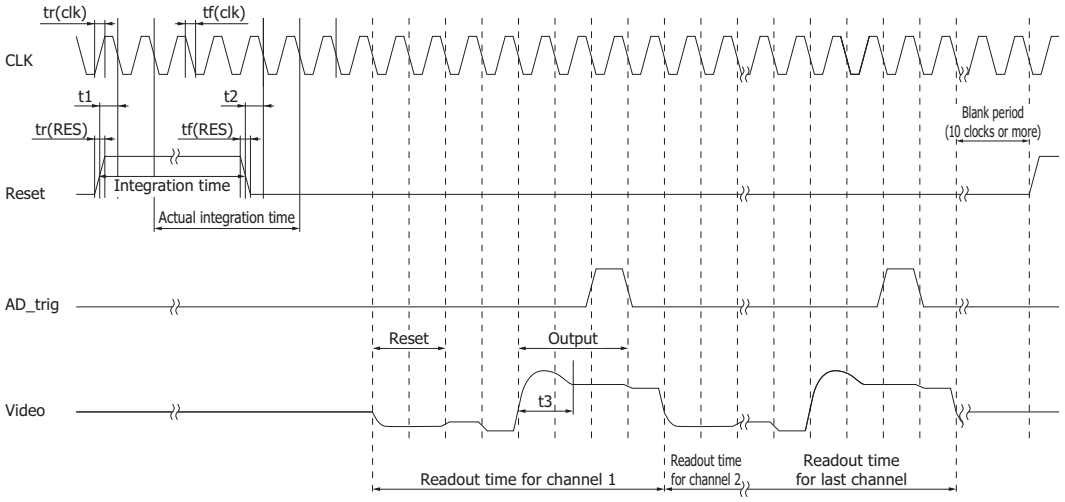
$$\begin{aligned} tscan &= (tc \times 14) + (tr \times N) \cdots\cdots\cdots\cdots\cdots\cdots (12) \\ &= 1\ [\mu s] \times 14 + 8\ [\mu s] \times 256 \\ &= 2062\ [\mu s] \end{aligned}$$

tc: CLK period
N: number of pixels

In this case, the reset time [low period of Reset in Figure 7-16 (a)] must be longer than the time required for one scan, so set the scan time (tscan) longer than 2062 µs. Note that the scan time becomes slightly

[Figure 7-16] Timing chart

(a) G9201 series



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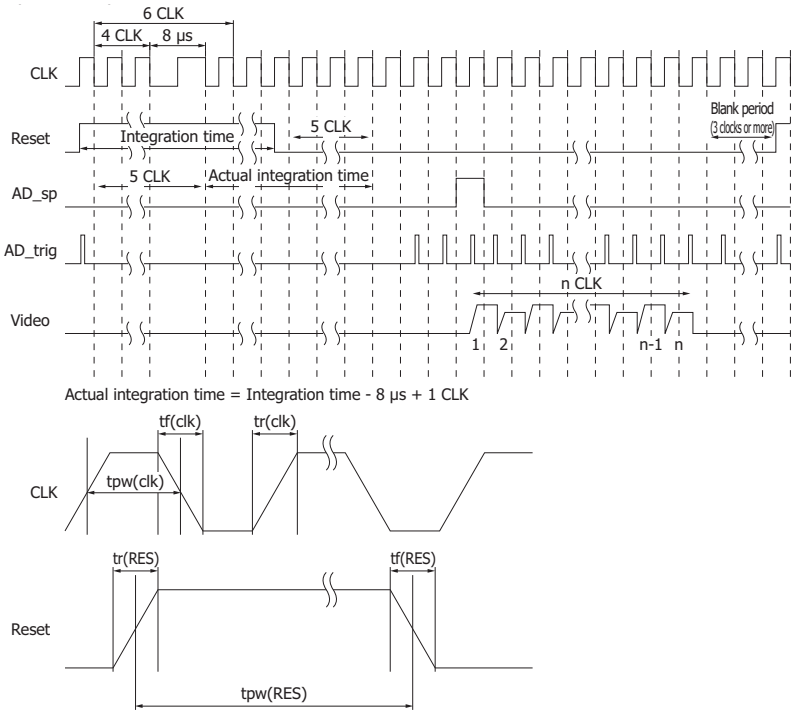
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f	0.1	-	4	MHz
Clock pulse width	tpw(clk)	100	-	-	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	100	ns
Reset pulse width	tpw(RES)	6000	-	-	ns
Reset pulse rise/fall times	tr(RES), tf(RES)	0	20	100	ns
Reset (rise) timing	t1	50	-	-	ns
Reset (fall) timing	t2	50	-	-	ns
Output settling time	t3	-	-	600	ns

(b) G11135 series



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Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency		f	0.1	-	5	MHz
Clock pulse width		tpw(clk)	60	100	-	ns
Clock pulse rise/fall times		tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	High	tpw(RES)	*1	-	*2	clock
	Low		Number of channels + 12	-	-	
Reset pulse rise/fall times		tr(RES), tf(RES)	0	20	30	ns

*1: (8 µs + 5 CLK) or (18 µs - 1 CLK), the longer of the two
*2: 1.008 ms - 1 CLK

longer depending on the Reset pulse width and the synchronization with the CLK signal.
The G9201 series performs simultaneous integration of all pixels and sequential readout, so the line rate is calculated from the integration time (high period of Reset) and the time required for one scan (tscan). Since the maximum CLK frequency is 4 MHz and the minimum integration time is 6 µs for the G9201 series, the maximum line rate of the G9201-256S is expressed by equation (13).

$$\text{Maximum line rate} = 1/(\text{Integration time} + \text{tscan}) \cdots\cdots (13)$$
$$= 1/(6\ [\mu s] + 515.5\ [\mu s])$$
$$= 1917\ [\text{lines/s}]$$

The longer the integration time, the lower the line rate.

- Example 2: When operating an InGaAs linear image sensor G11135-512DE at a CLK frequency of 5 MHz

Since the video signal readout frequency equals the CLK signal frequency, the readout time (tr) per pixel is 0.2 µs. The time (tscan) required for one scan is therefore given by equation (14).

$$\text{tscan} = (\text{tc} \times 12) + (\text{tr} \times \text{N}) \cdots\cdots (14)$$
$$= 0.2\ [\mu s] \times 12 + 0.2\ [\mu s] \times 512$$
$$= 104.8\ [\mu s]$$

tc: CLK period
N: number of pixels

The reset time must be longer than the scan time, so set the reset time longer than 104.8 µs. Note that the scan time becomes slightly longer depending on the Reset signal's pulse width and the synchronization with the CLK signal.
The G11135 series performs simultaneous integration of all pixels and sequential readout, so the line rate is calculated from the integration time (high period of Reset) and the time required for one scan (tscan). Since the maximum CLK frequency is 5 MHz and the minimum integration time is 17.8 µs for the G11135 series, the maximum line rate of the G11135-512DE is expressed by equation (15).

$$\text{Maximum line rate} = 1/(\text{integration time} + \text{tscan}) \cdots\cdots (15)$$
$$= 1/(17.8\ [\mu s] + 104.8\ [\mu s])$$
$$= 8156\ [\text{lines/s}]$$

The longer the integration time, the lower the line rate.

(4) Turning on the power supply for the thermoelectric cooler

Use extra caution to avoid damaging the image sensor when turning on the power to the thermoelectric cooler. Take the following precautions when designing a power supply circuit for the thermoelectric cooler.

- Never exceed the absolute maximum ratings for the thermoelectric cooler.
- Make sure that the power supply voltage and connection polarity are correct. Turning on the power supply with the wrong voltage or polarity will damage the image sensor.
- A power supply with the lowest possible noise and ripple should be used. Also, use power supply wires thick enough to keep impedance as low as possible. The TE+ and TE- wires in particular must be sufficiently thick.
- Be sure to provide an over-current safeguard circuit to protect the thermoelectric cooler from being damaged.
- Provide a protection circuit that monitors the temperature on the heat-emitting side of the heatsink to prevent the heatsink temperature from exceeding the specified level due to excessive cooling.
- While referring to Figures 7-13 and 7-14, set the optimum voltage and current values that maintain the target temperature.

7 - 6 New approaches

InGaAs image sensors are widely used for near infrared spectrophotometry. When a sample is irradiated with near infrared light, it reflects or transmits the light. A characteristic spectrum is obtained by separating the reflecting or transmitting diffused light into individual wavelengths. This spectrum contains multiple pieces of information regarding the components of the sample, so measuring this spectrum allows for rapid, non-destructive quantitative/qualitative analysis. Near infrared spectrometers have been downsized and are widely used not only in laboratories but also on production lines or in outdoor locations.
This expanded field of applications means that infrared image sensors will need higher cost performance. Meeting this requirement will require fabricating larger wafers and smaller chips in order to yield a greater number of chips from one wafer.

To solve this challenging problem, back-illuminated structures will help reduce the chip size as well as decrease the wiring capacitance to achieve higher speeds. In the future, the development of a narrow-pitch charge amplifier array will help suppress output variations caused by differences in the video line, which have long been a problem with conventional devices. In addition, we will make InGaAs image sensors which improved the sensitivity in the short wavelength region, enabling light detection over a wide range from the visible region to the near infrared region.

8. InGaAs area image sensors

InGaAs area image sensors detect near infrared rays invisible to the human eye and convert the weak light into images. They have a hybrid structure consisting of a two-dimensional back-illuminated InGaAs photodiode array and high-gain low-noise CMOS readout circuit (ROIC: readout integrated circuit) that are connected by In bumps. A pixel is made up of one InGaAs photodiode element and one ROIC. The ROIC has a built-in timing generator that makes it possible to produce analog video outputs and AD_trig digital outputs with a simple application of an external master clock (MCLK) and master start pulse (MSP).

8 - 1 Features

- Cutoff wavelength: 1.7 µm or 1.9 µm
- High quantum efficiency
- High sensitivity: 1 µV/e^- min.
- Readout mode: Global shutter mode, rolling shutter mode
- Simple operation: built-in timing generator
- Hermetic seal package: compact, high reliability

8 - 2 Structure

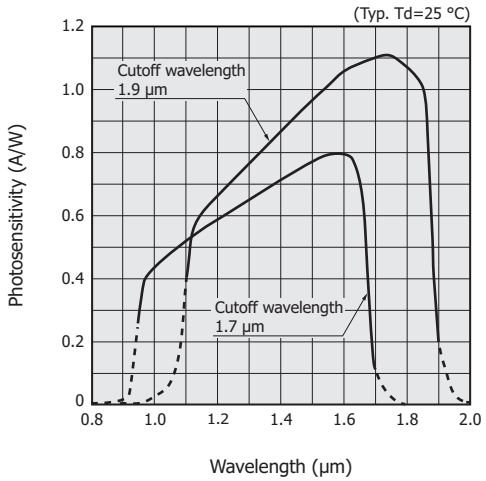
InGaAs photodiode

The two-dimensional back-illuminated InGaAs photodiode array built into the InGaAs area image sensor provides high quantum efficiency in the near infrared region [Figure 8-1]. We also offer a type with built-in thermoelectric cooler for controlling the photodiode temperature.

[Table 8-1] Hamamatsu InGaAs area image sensors

Type	Cutoff wavelength (µm)	Number of pixels	Pixel pitch (µm)	ROIC	Cooling	Package
Wide dynamic range, compact	1.7	64 × 64	50	CTIA	One-stage TE-cooled	TO-8
Wide dynamic range		128 × 128				28L metal
Long wavelength, compact	1.9	64 × 64			Two-stage TE-cooled	TO-8
High resolution, compact	1.7	128 × 128	20	SF	Two-stage TE-cooled	TO-8
High resolution (VGA)		640 × 512				28L metal

[Figure 8-1] Spectral response



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ROIC

The ROIC in the InGaAs area image sensor is manufactured to suit the characteristics of the InGaAs photodiode using CMOS technology. Multi-functionality and high performance as well as cost reduction in constructing systems are accomplished by mounting the analog circuit for signal processing and the digital circuit for generating timing signals on a single chip.

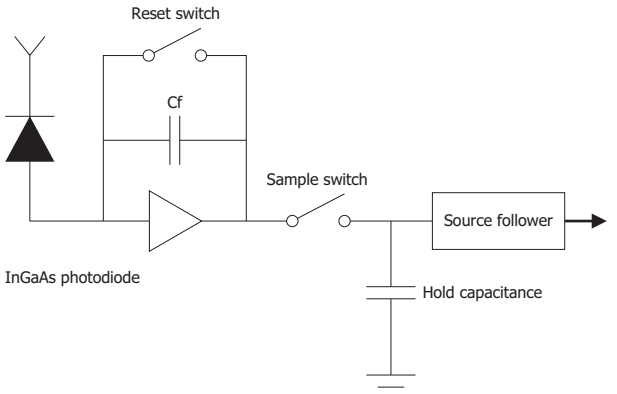
The ROIC comes in two types: CTIA (capacitive trans-impedance amplifier) and SF (source follower). The proper ROIC type must be selected according to the application. Figure 8-2 shows block diagrams of each type.

The advantages of the CTIA type are that (1) the charge-to-voltage converter takes on an amplifier structure and (2) it has superior linearity since the voltage applied to the InGaAs photodiodes can be kept constant. The disadvantages are that (1) the power consumption by the amplifier is large and (2) temperature control using the TE-cooler is necessary because of the temperature increase in the sensor caused by the large power consumption. In addition, with the CTIA type, the pitch is larger because the size of the amplifier is larger than that of the SF type.

The SF type provides high gain and high resolution. Since the charge-to-voltage converter has a simple structure and is small, the pitch can be made smaller and higher mounting density is possible. In addition, it does not require cooling due to its low power consumption. Moreover, high sensitivity can be attained because the parasitic capacitance can be reduced. The disadvantage is its narrow linearity range.

[Figure 8-2] Block diagram

(a) CTIA type



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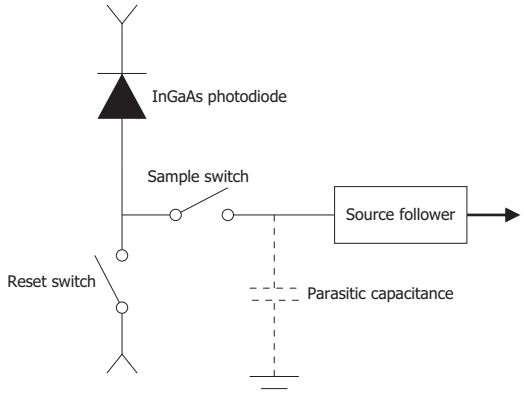
(b) SF type



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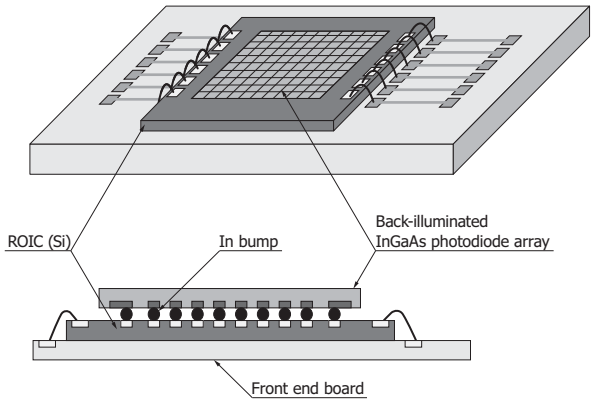
There are two signal readout modes: global shutter mode and rolling shutter mode. In global shutter mode, all pixels are reset simultaneously, and integration of all pixels begin at the same time. Therefore, data integrated over the same time duration is output from all pixels. In rolling shutter mode, a reset occurs every line, the data is output, and then integration starts immediately. If you want to prioritize the frame rate, select the rolling shutter mode.

In (indium) bumps

In bumps electrically connect the InGaAs photodiode and ROIC. Since the Young's modulus of In is lower than that of Au, Cu, and Al and the melting point is 157 °C, distortion caused by heat can be suppressed. Thus, In is suitable for connecting metals and semiconductors with different thermal expansion coefficients.

[Figure 8-3] Schematic of InGaAs area image sensor



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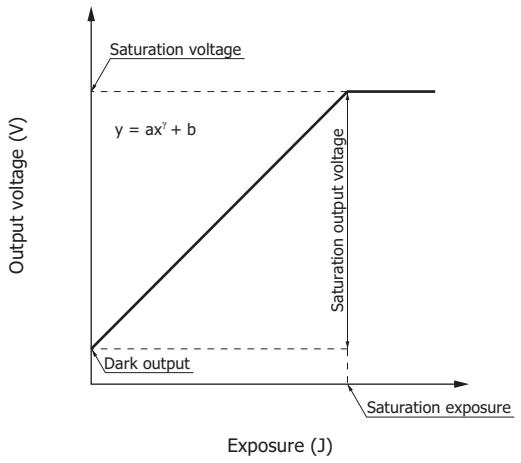
8 - 3 Characteristics

Input/output characteristics

The input/output characteristics express the relation between the light level incident to the image sensor and the signal output. Since InGaAs area image sensors operate in charge amplifier mode, the incident light exposure (unit: J) is expressed by the product of light level (unit: W) and integration time (unit: s). Figure 8-4 shows a schematic diagram of the input/output characteristics. The slope in the figure can be expressed by equation (1).

[Figure 8-4] Schematic graph of input/output characteristics (log graph)



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$$y = ax^{\gamma} + b \quad \cdots\cdots\cdots (1)$$

y: output voltage
a: sensitivity (ratio of output with respect to the exposure)
x: exposure
γ: slope coefficient
b: dark output (output when exposure=0)

Since the upper limit of the output voltage is determined by the output voltage range of the ROIC, the input/output characteristics will have an inflection point. The incident light exposure at this inflection point is referred to as the saturation exposure, the output voltage as the saturation output voltage, and the amount of charge stored in the charge amplifier as the saturation charge.

In our InGaAs linear image sensor datasheets, the saturation output voltage (Vsat) is defined as the saturated output voltage from light input minus the dark output. The saturation charge is calculated from the equation Q = C V based on the saturation output voltage. If the integration capacitance (Cf) is 0.1 pF and the saturation output voltage is 2.0 V, then the saturation charge will be 0.2 pC.

Photoresponse nonuniformity

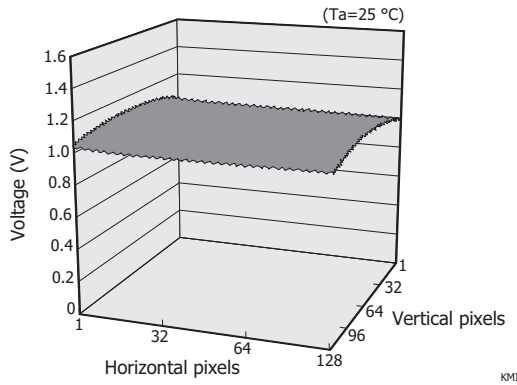
InGaAs area image sensors contain a large number of InGaAs photodiodes arranged in an array, yet sensitivity of each photodiode (pixel) is not uniform. This may result from crystal defects in the InGaAs substrate and/or variations in the processing and diffusion in the manufacturing process as well as inconsistencies in the ROIC gain. For our InGaAs area image sensors, variations in the outputs from all pixels measured when the effective photosensitive area of each photodiode is uniformly illuminated are referred to as photoresponse nonuniformity (PRNU) and defined as shown in equation (2).

$$PRNU = (\Delta X/X) \times 100\ [\%] \quad \cdots\cdots\cdots (2)$$

X : average output of all pixels
ΔX: absolute value of the difference between the average output X and the output of the maximum (or minimum) output pixel

In our outgoing product inspection for photoresponse nonuniformity, the output is adjusted to approx. 50% of the saturation output voltage and a halogen lamp is used as the light source. Since InGaAs area image sensors use a compound semiconductor crystal for photoelectric conversion, the photodiode array may contain crystal defects, resulting in abnormal output signals from some of the pixels (defective pixels). Moreover, scratches and stain on the light input window may also cause the sensitivity uniformity to deteriorate. So caution should be exercised on this point when handling image sensors. Figure 8-5 shows typical example of photoresponse nonuniformity (random sampling).

[Figure 8-5] Photoresponse nonuniformity (G12242-0707W, typical example)



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Dark output

The dark output is the output generated even when no incident light is present. This output is the sum of the dark current (sum of diffusion current, recombination current, and surface leakage current) of the photodiode and the ROIC offset voltage. Since the upper limit of the video output is determined by the saturation output voltage, a large dark output narrows the dynamic range of the output signal. The output signal is the sum of the output generated by light and the dark output, so the purity of the output signal can be improved by using signal processing to subtract the dark output from each pixel. The dark output is given by equation (3). The integration time must be determined by taking the magnitude of the dark output into account.

$$Vd = I_D \times (Ts/Cf) + Voff \cdots\cdots (3)$$

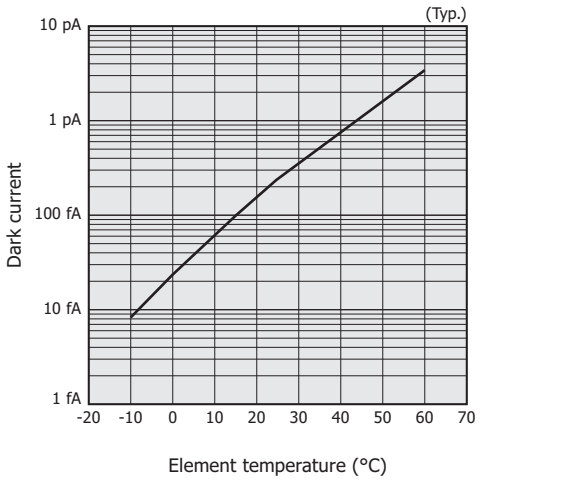
Vd : dark output [V]
I_D : dark current [pA]
Ts : integration time [s]
Cf : integration capacitance [pF]
Voff: ROIC offset voltage [V]

The band gap widens as the temperature decreases, so the number of carriers thermally excited into the valence band from the conduction band decreases, causing the dark current to reduce exponentially. In our InGaAs area image sensors, the temperature coefficient β of the dark current is 1.06 to 1.1. If the dark current at temperature T_1 (unit: °C) is I_{DT1} (unit: A), then the dark current I_{DT} at temperature T is expressed by equation (4).

$$I_{DT} = I_{DT1} \times \beta^{(T - T_1)} \text{ [A]} \cdots\cdots (4)$$

Figure 8-6 shows the temperature characteristics of the G12242-0707W dark current (random sampling).

[Figure 8-6] Temperature characteristics of dark current (G12242-0707W)



Noise

InGaAs area image sensor noise can be largely divided into fixed pattern noise and random noise. Fixed pattern noise includes ROIC DC offset voltage and photodiode dark current which is current noise from the DC component. The magnitude of the fixed pattern noise is constant even if readout conditions are changed, so it can be canceled by using an external signal processing circuit.
Random noise, on the other hand, results from fluctuations in voltage, current, or charge that are caused in the signal output process in the sensor. When the fixed pattern noise has been canceled by external signal processing, the random noise will then determine the InGaAs area image sensor's detection limit for low-level light or lower limit of dynamic range. Random noise includes the following four components:

① Dark current shot noise (Nd)
② Signal current shot noise at light input (Ns)
③ Charge amplifier reset noise (Nr)
④ CMOS charge amplifier readout noise (N_R)

Dark current shot noise ① results from erratic fluctuation in charge. This noise becomes larger as the output charge due to dark current increases, and therefore varies depending on operating conditions such as integration time and temperature. Signal current shot noise ② is caused by fluctuations due to incident photons arriving randomly at the sensor. The total noise (N) is expressed by equation (5).

$$N = \sqrt{Nd^2 + Ns^2 + Nr^2 + N_R^2} \cdots\cdots (5)$$

We specify the noise level (unit: V rms) in InGaAs area image sensors as fluctuations in the output voltage of each pixel.

8 - 4 New approaches

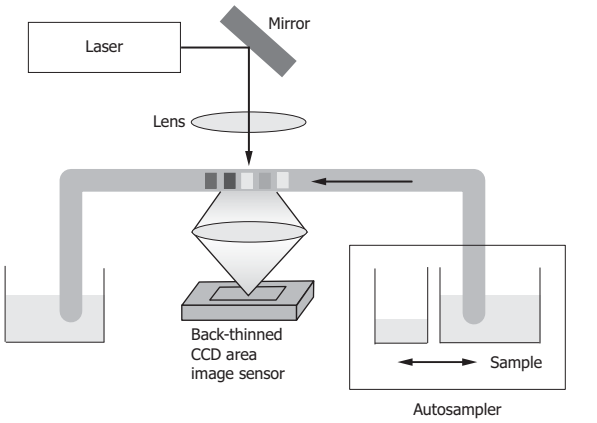
InGaAs area image sensors used for infrared detection significantly increase the information obtained through detection as compared to single-element InGaAs PIN photodiodes or InGaAs linear image sensors. Its field of application is expanding including night vision for security purposes, plastic sorting (pet bottles and other disposables), farm produce sorting (e.g., grains), semiconductor analyzers, and academic research (astronomy and satellite). Night vision and semiconductor analyzers require detection of low level emissions from the object with high reproducibility. This requires high sensitivity and high resolution, which must be accomplished by increasing the conversion gain and decreasing the pitch at the same time. Hamamatsu is working to optimize the ROIC and developing fine pitch bump bonding. Sorters use different wavelengths depending on the object. Long wavelength is used in farm produce sorting, and high-speed processing is also required. Hamamatsu will increase the area of long wavelength type InGaAs area image sensors and achieve high-speed processing by increasing the speed of buffer amplifiers and using multiple ports.

9. Applications

9 - 1 DNA sequencers

Here we introduce the DNA sequencer, which is one typical application for back-thinned CCDs. The DNA sequencer uses laser light to excite DNA fragments labeled with fluorescent dye and separated according to molecular weight, and then sequentially reads out their base sequence by detecting the resulting fluorescent light.
The DNA sequencer must be able to detect the faint fluorescent light representing the four DNA bases (adenine, thymine, cytosine, and guanine) with good accuracy, and it utilizes back-thinned CCDs having high quantum efficiency close to the detection limit in the visible light range.

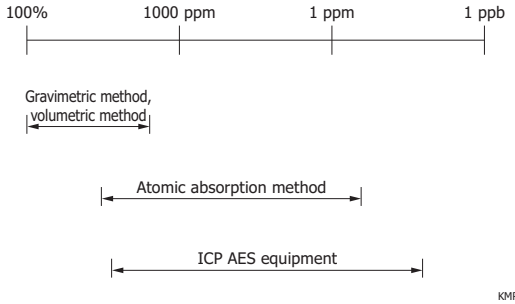
[Figure 9-1] Configuration of DNA sequencer



9 - 2 ICP AES equipment

The ICP AES (inductively coupled plasma atomic emission spectroscopy) equipment performs qualitative and quantitative analysis of trace metals within a liquid. The demand for ICP AES equipment is increasing rapidly as an effective means of making environmental measurements.
ICP AES equipment requires high detection sensitivity and accuracy, and therefore uses back-thinned CCDs with low noise and high sensitivity. The spectral range to be detected partly includes ultraviolet light, so our back-thinned CCDs with high ultraviolet sensitivity are found beneficial in enhancing the sensitivity of ICP AES equipment.

[Figure 9-2] Sensitivity comparison between various types of analytical technique



9 - 3 Optical emission spectrometers

The optical emission spectrometer (OES) applies energy to samples in various ways and performs spectroscopic analysis on the emitted light to qualitatively and quantitatively analyze the sample components. The emitted light spectrum varies depending on the elements contained in the sample and spans from the ultraviolet region to the near infrared region. Hamamatsu back-thinned CCD linear image sensors feature high UV sensitivity suitable for OES.

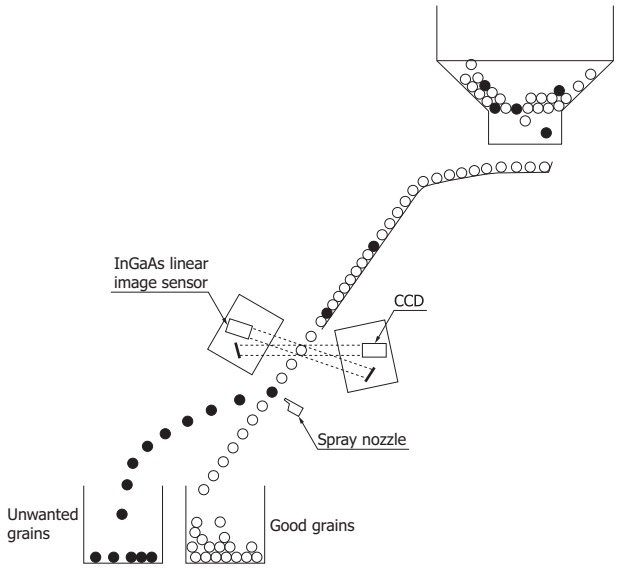
9 - 4 Spectrophotometers

The S9971 series of front-illuminated CCD with an internal thermoelectric cooler is used in spectrophotometry over a broad spectral range (400 to 1200 nm). The S9971 series is low cost compared to back-thinned CCDs with the same photosensitive area size, making it suitable as a sensor in compact spectrophotometers.
Back-thinned CCD area image sensors with high sensitivity from the ultraviolet region to near infrared region can be used as linear image sensors of vertically long pixels during binning. Since these sensors are highly sensitive over a wide spectral range and have a sensor structure suitable for spectrophotometers, they are used in a variety of spectrophotometers that require highly accurate measurements such as LED testers and light interference type thickness meters for semiconductor process monitoring.
We also provide PMA (photonic multichannel analyzer) and mini-spectrometers that incorporate our CCD image sensors or InGaAs linear image sensors.

9 - 5 Grain sorters

Grain sorters irradiate light onto the falling grain, identify unwanted items from the reflected or transmitted light, and then remove those from the grain by high-pressure air spray. Using InGaAs linear image sensors in the grain sorter allows simultaneously identifying multiple grain types while analyzing grain components.

[Figure 9-3] Schematic of grain sorter



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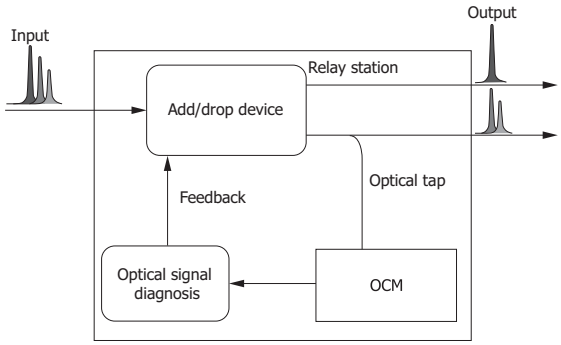
9 - 6 Optical channel monitors

Devices called optical channel monitors (OCM) fulfill an important role in monitoring the signal wavelength and power on wavelength division multiplexing (WDM) networks that carry huge quantities of information. InGaAs linear image sensors used in the OCM detect light spatially separated by spectral-dispersion elements.

[Figure 9-4] Schematic of optical channel monitor



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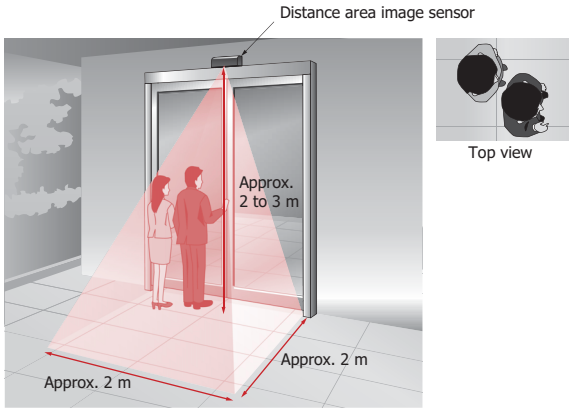
9 - 7 Security and room access control, obstacle detection, and shape recognition

The light from a light source is incident on the subject, and a distance image sensor detects the reflected light. The distance to the subject is then calculated using the TOF (time-of-flight) method. The distance measurement system combined with image processing is a promising device for use in security and room access control (tailgate detection), obstacle detection (unmanned vehicles, robots, etc.), shape recognition (logistics, robots, etc.), and motion capture.

[Figure 9-5] Security (tailgate detection)



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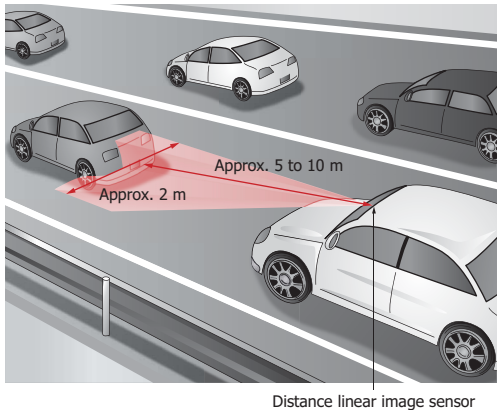
[Figure 9-6] Obstacle detection by automobiles



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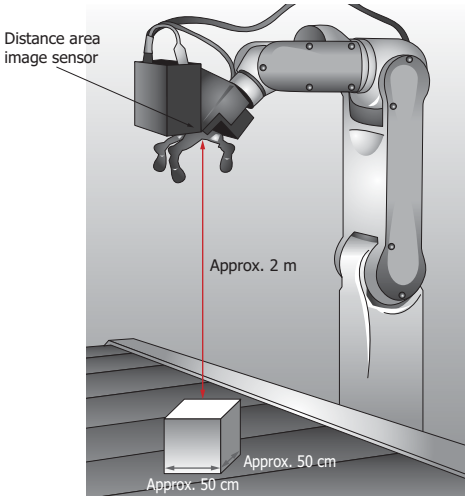
[Figure 9-7] Shape recognitions by robot



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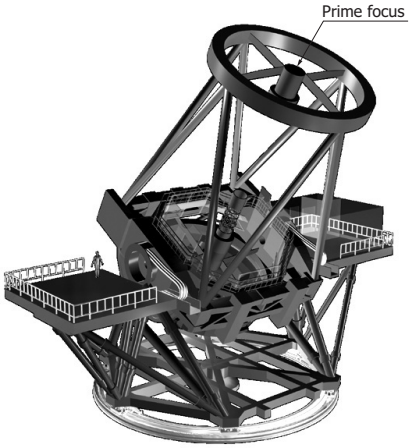
9 - 8 Detector for prime focus camera of Subaru Telescope

The near infrared-enhanced back-illuminated CCD (fully-depleted CCD with thick silicon) is being used as a detector for the prime focus camera of the Subaru Telescope (National Astronomical Observatory of Japan) that is installed on the top of Mauna Kea on the island of Hawaii. This CCD featuring high quantum efficiency at 1000 nm is expected to contribute greatly in the leading field of observational astronomy, such as in the research of dark energy and distant space (e.g., discovery of the first heavenly body created in the universe).

In 2008, Suprime-Cam containing ten of our CCDs (S10892-01) began its operation. In 2013, observation using Hyper Suprime-Cam began. It uses 116 CCDs (S10892-02) with improved sensitivity in the blue region. This CCD not only has high sensitivity from the visible region to the 1000 nm near infrared region but also in the soft X-ray region (up to 20 keV). Due to its superior performance, this CCD has already be chosen to be used in Japan's X-ray astronomical satellite ASTRO-H.

[Figure 9-8] Subaru Telescope



(Courtesy of National Astronomical Observatory of Japan)

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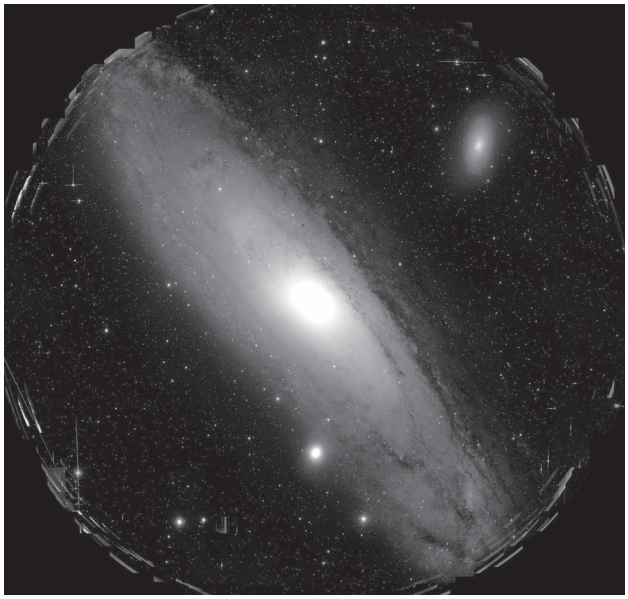
[Figure 9-9] Andromeda galaxy captured by the Subaru Telescope



9 - 9 Asteroid explorer Hayabusa

Hamamatsu CCD area image sensor was chosen as the detector of the Hayabusa's fluorescent X-ray spectrometer (a device for investigating materials on the surface of the asteroid from above). Elements in matter on the ground emit fluorescent X-rays of a certain wavelength in response to energy from X-rays from the sun. The wavelengths of the fluorescent X-rays are defined for each element, so, by measuring the fluorescent X-rays emitted from the surface of an asteroid, it is possible to determine about how much of what elements are there. The fluorescent X-ray spectrometer succeeded in measuring the material composition of the asteroid Itokawa's surface, which included magnesium, aluminum, silicon, etc.

In addition, our InGaAs linear image sensor was chosen for the Hayabusa's near-infrared spectrometer owing to the sensor's high sensitivity in the near-infrared region as well as its high reliability and durability. The near-infrared spectrometer (NIRS) on Hayabusa was a device to disperse and detect infrared rays from the sunlight reflected off the surface of the asteroid, in order to analyze the minerals on the ground and the form of the terrain. When 0.8 to 2.1 μm light reflected from Itokawa was spectroscopically measured, it was found that reflectance dropped at the regions of 1 μm and 2 μm. Thus, it was concluded that the minerals on the surface include olivine and pyroxene.

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