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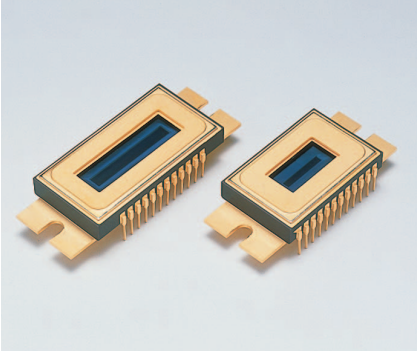
CCD area image sensor



S10140/S10141 series

Low readout noise, high resolution (pixel size: 12 µm)

The S10140/S10141 series is a family of back-thinned FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, the S10140/S10141 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes the S10140/S10141 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S10140/S10141 series also features low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
The S10140/S10141 series has an effective pixel size of 12 × 12 µm and is available in image areas ranging from 12.288 (H) × 1.464 (V) mm^2 (1024 × 122 pixels) up to a large image area of 24.576 (H) × 6.072 (V) mm^2 (2048 × 506 pixels).

Features

- **Low readout noise: 4 e$^-$ rms typ.**
- **High resolution: pixel size 12 × 12 µm**
- **Non-cooled type: S10140 series**
  One-stage TE-cooled type: S10141 series
- **Line, pixel binning, area scanning**
- **Greater than 90% quantum efficiency at peak sensitivity wavelength**
- **Wide spectral response range**
- **Wide dynamic range**
- **MPP operation**
- **High UV sensitivity with good stability**
- **Same pin connections as S7030/S7031 series**

Applications

- **Fluorescence spectrometer, ICP**
- **Industrial inspection requiring**
- **Semiconductor inspection**
- **DNA sequencer**
- **Low-light-level detection**
- **Raman spectroscopy**

Selection guide

Type no.	Cooling	Number of total pixels	Number of effective pixels	Image size [mm (H) × mm (V)]	Suitable multichannel detector head
S10140-1007	Non-cooled	1044 × 128	1024 × 122	12.288 × 1.464	C10150
S10140-1008		1044 × 256	1024 × 250	12.288 × 3.000	
S10140-1009		1044 × 512	1024 × 506	12.288 × 6.072	
S10140-1107		2068 × 128	2048 × 122	24.576 × 1.464	
S10140-1108		2068 × 256	2048 × 250	24.576 × 3.000	
S10140-1109		2068 × 512	2048 × 506	24.576 × 6.072	
S10141-1007S	One-stage TE-cooled	1044 × 128	1024 × 122	12.288 × 1.464	C10151
S10141-1008S		1044 × 256	1024 × 250	12.288 × 3.000	
S10141-1009S		1044 × 512	1024 × 506	12.288 × 6.072	
S10141-1107S		2068 × 128	2048 × 122	24.576 × 1.464	
S10141-1108S		2068 × 256	2048 × 250	24.576 × 3.000	
S10141-1109S		2068 × 512	2048 × 506	24.576 × 6.072	

Note: Two-stage TE-cooled type (S7032-1006/-1007) is available upon request (made-to-order product).

Structure

Parameter	S10140 series	S10141 series
Pixel size (H × V)	12 × 12 µm	
Vertical clock phase	2 phases	
Horizontal clock phase	2 phases	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outlines)	
Window*1	Quartz glass*2	AR-coated sapphire*3

*1: Temporary window type (ex. S10140-1107N) is available upon request.
*2: Resin sealing
*3: Hermetic sealing

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*4	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	V_{OD}	-0.5	-	+30	V
Reset drain voltage	V_{RD}	-0.5	-	+18	V
Vertical input source voltage	V_{ISV}	-0.5	-	+18	V
Horizontal input source voltage	V_{ISH}	-0.5	-	+18	V
Vertical input gate voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
Horizontal input gate voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
Summing gate voltage	V_{SG}	-10	-	+15	V
Output gate voltage	V_{OG}	-10	-	+15	V
Reset gate voltage	V_{RG}	-10	-	+15	V
Transfer gate voltage	V_{TG}	-10	-	+15	V
Vertical shift register clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
*4: Package temperature (S10140 series), chip temperature (S10141 series)

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	23	24	25	V
Reset drain voltage			V_{RD}	11	12	13	V
Output gate voltage			V_{OG}	2.5	3	3.5	V
Substrate voltage			V_{SS}	-	0	-	V
Test point	vertical input source		V_{ISV}	-	V_{RD}	-	V
	horizontal input source		V_{ISH}	-	V_{RD}	-	V
	vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	V
	horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	V
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	2.5	3	3.5	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	4	5	6	V
		Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	4	5	6	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	4	5	6	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	2.5	3	3.5	V
		Low	V_{TGL}	-9	-8	-7	
External load resistance			R_L	90	100	110	kΩ

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	250	500	kHz
Vertical shift register capacitance	S1014*-1007	C_{P1V}, C_{P2V}	-	800	-	pF
	S1014*-1008/-1107		-	1600	-	
	S1014*-1108/-1009		-	3200	-	
	S1014*-1109		-	6400	-	
Horizontal shift register capacitance	S1014*-1007/-1008/-1009	C_{P1H}, C_{P2H}	-	80	-	pF
	S1014*-1107/-1108/-1109		-	150	-	
Summing gate capacitance		C_{SG}	-	30	-	pF
Reset gate capacitance		C_{RG}	-	30	-	pF
Transfer gate capacitance	S1014*-1007/-1008/-1009	C_{TG}	-	50	-	pF
	S1014*-1107/-1108/-1109		-	70	-	
Charge transfer efficiency*5		CTE	0.99995	0.99999	-	-
DC output level*6		Vout	16	17	18	V
Output impedance*6		Zo	-	8	-	kΩ
Power consumption*6 *7		P	-	4	-	mW

*5: Charge transfer efficiency per pixel, measured at half of the full well capacity
*6: The values depend on the load resistance. (Typ. V_{OD}=24 V, Load resistance=100 kΩ)
*7: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

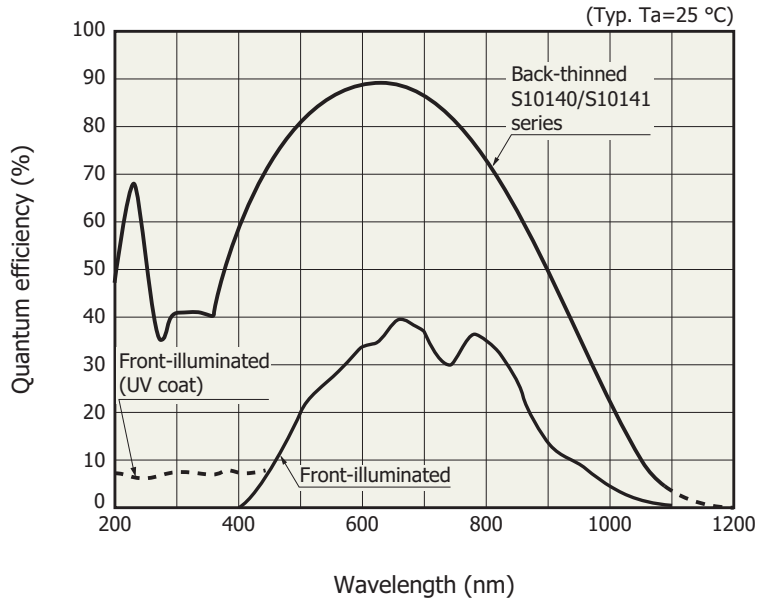
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical		Fw	45	60	-	ke^-
	Horizontal			120	150	-	
	Summing			150	200	-	
CCD node sensitivity			Sv	4	5	6	$\mu V/e^-$
Dark current*8 MPP mode	25 °C		DS	-	30	300	e^-/pixel/s
	0 °C			-	3	30	
Readout noise*9			Nr	-	4	18	e^- rms
Dynamic range*10	Line binning		DR	30000	37500	-	-
	Area scanning			11250	15000	-	-
Photoresponse nonuniformity*11			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*12	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect*13			-	-	3	-
	Column defect*14			-	-	0	-

*8: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*9: -50 °C, operating frequency=20 kHz.
*10: Dynamic range = Full well/Readout noise
*11: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

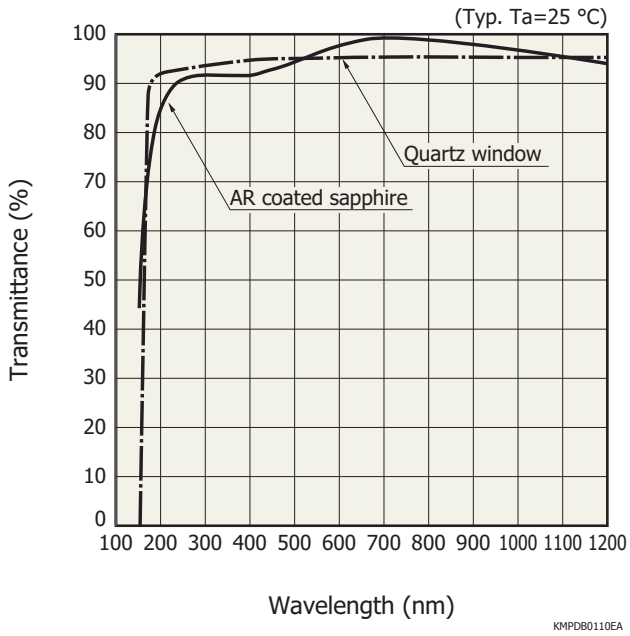
*12: White spots
Pixels whose dark current is higher than 1 ke^- after one-second integration at 0 °C.
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)
*13: 2 to 9 contiguous defective pixels
*14: 10 or more contiguous defective pixels

Spectral response (without window)*15

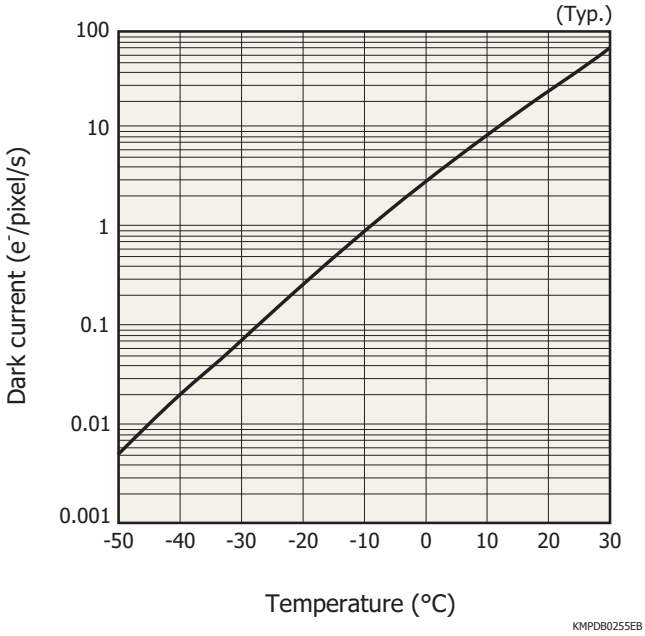


*15: Spectral response with quartz glass or AR-coated sapphire are decreased according to the spectral transmittance characteristics of window material.

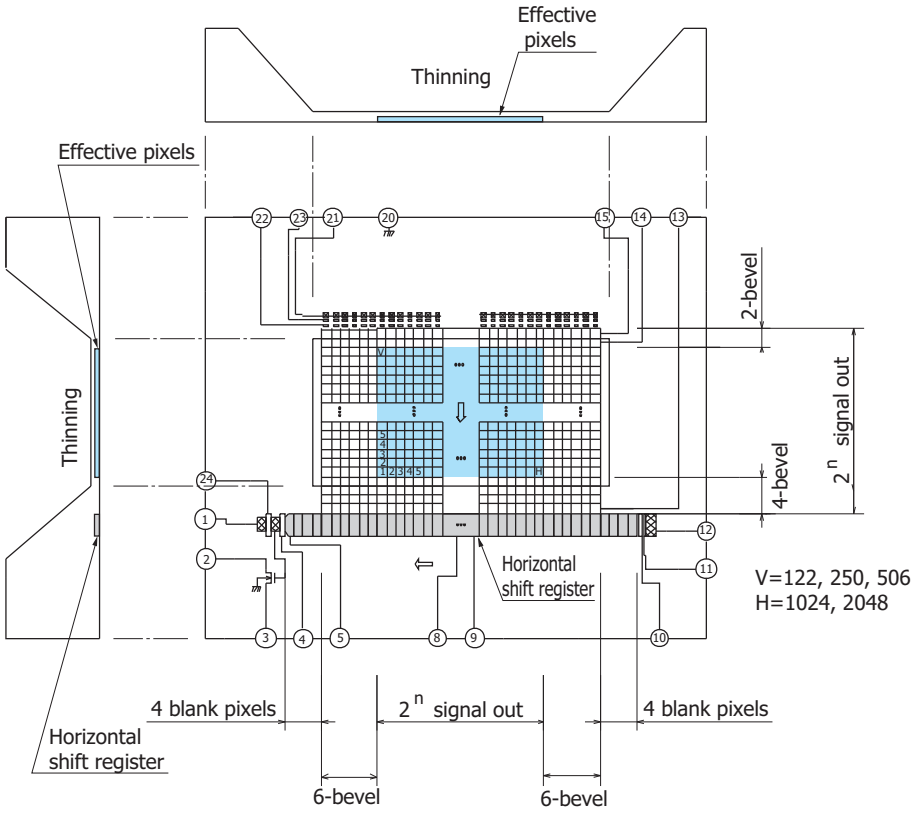
Spectral transmittance characteristics



Dark current vs. temperature



Device structure (conceptual drawing of top view)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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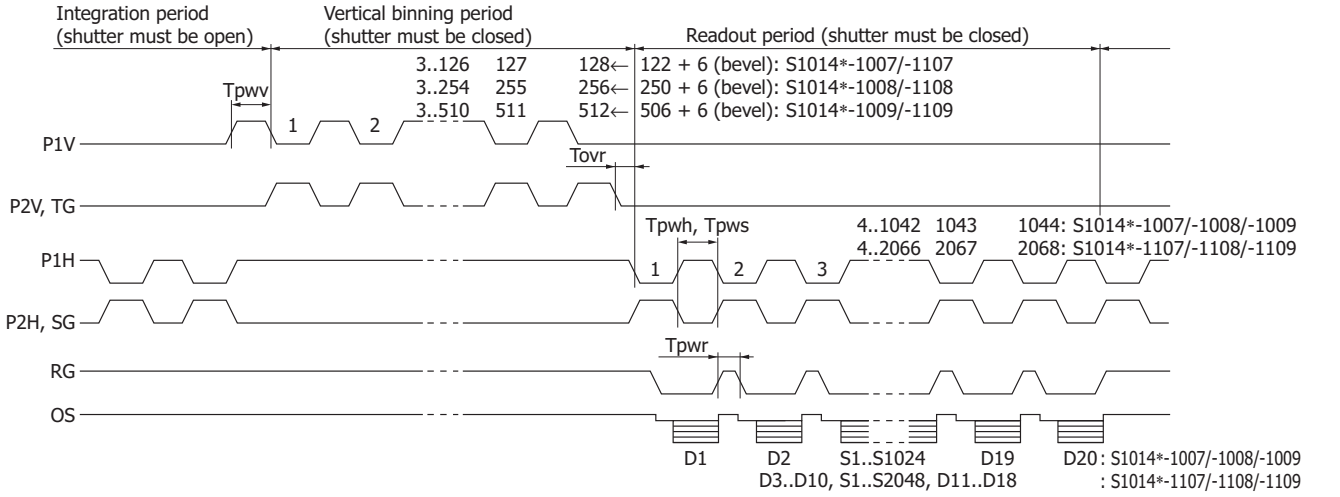
Timing chart

Line binning



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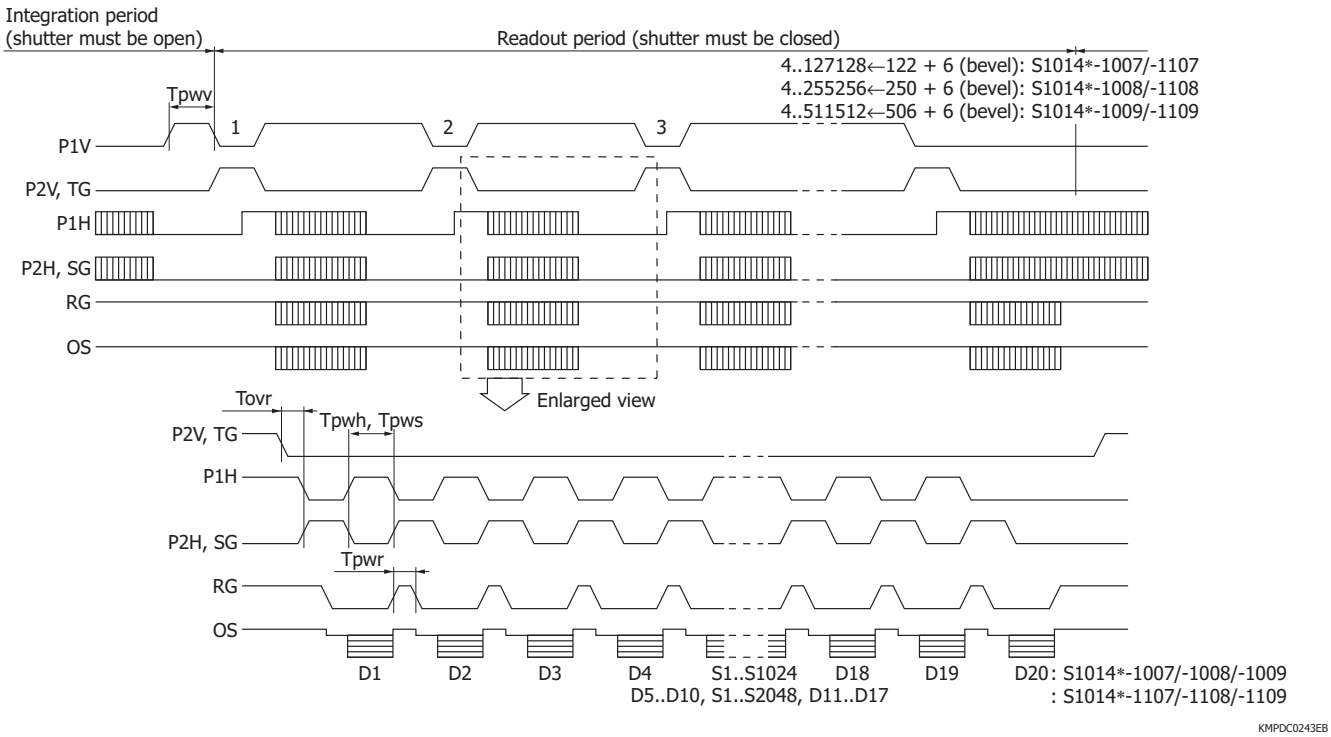
Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*16	Pulse width	S1014*-1007	Tpwv	1.5	2	-	µs
		S1014*-1008/-1107		3	4	-	
		S1014*-1009/-1108		6	8	-	
		S1014*-1109		12	16	-	
	Rise and fall times		Tprv, Tpfv	20	-	-	ns
P1H, P2H*16	Pulse width		Tpwh	1000	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	40	50	60	%
SG	Pulse width		Tpws	1000	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	40	50	60	%
RG	Pulse width		Tpwr	100	1000	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG – P1H	Overlap time		Tovr	1	2	-	µs

*16: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Area scanning

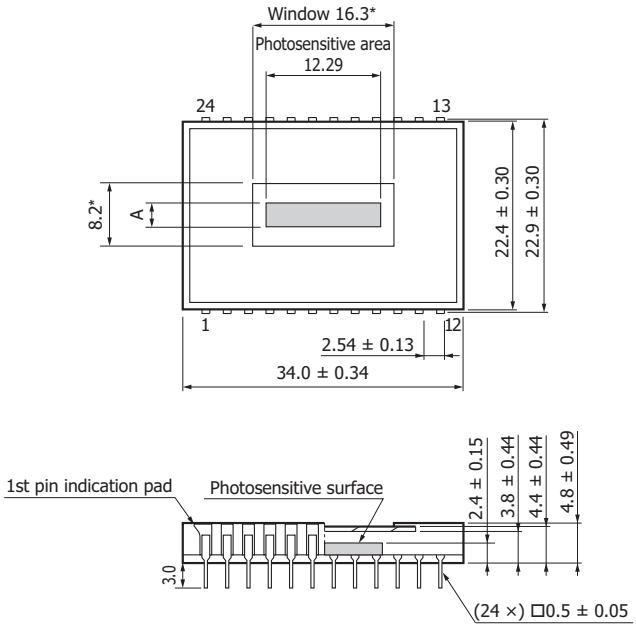


Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*17	Pulse width	S1014*-1007	Tpwv	1.5	2	-	µs
		S1014*-1008/-1107		3	4	-	
		S1014*-1009/-1108		6	8	-	
		S1014*-1109		12	16	-	
	Rise and fall times		Tprv, Tpfv	20	-	-	ns
P1H, P2H*17	Pulse width		Tpwh	1000	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	40	50	60	%
SG	Pulse width		Tpws	1000	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	40	50	60	%
RG	Pulse width		Tpwr	100	1000	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG – P1H	Overlap time		Tovr	1	2	-	µs

*17: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

S10140-1007/-1008/-1009



S10140-1007: A=1.464
S10140-1008: A=3.000
S10140-1009: A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph.

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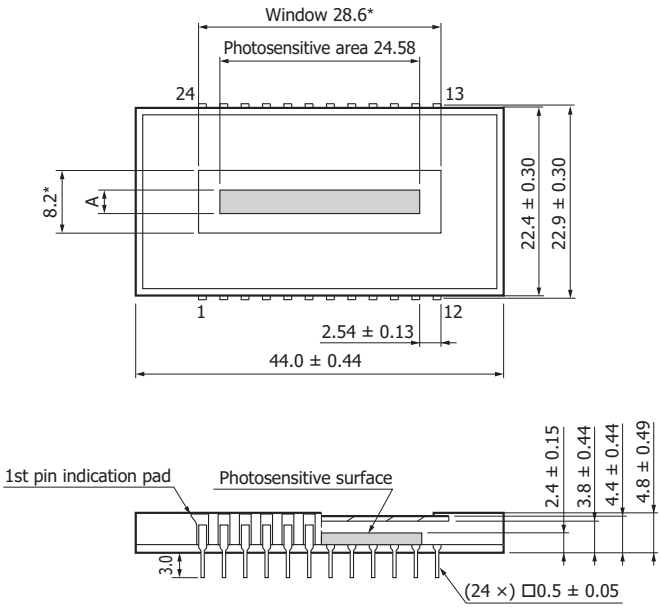
S10140-1107/-1108/-1109



S10140-1107: A=1.464
S10140-1108: A=3.000
S10140-1109: A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph.

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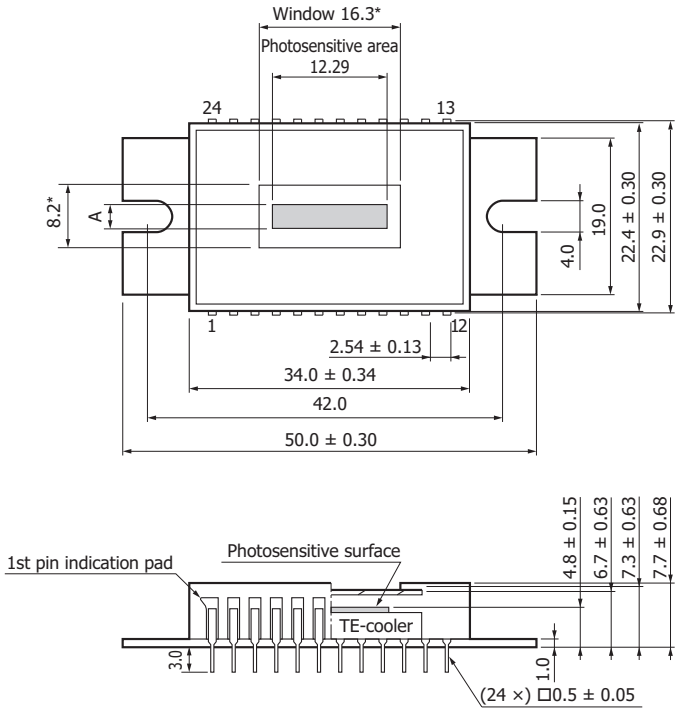
S10141-1007S/-1008S/-1009S



S10141-1007S: A=1.464
S10141-1008S: A=3.000
S10141-1009S: A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph.

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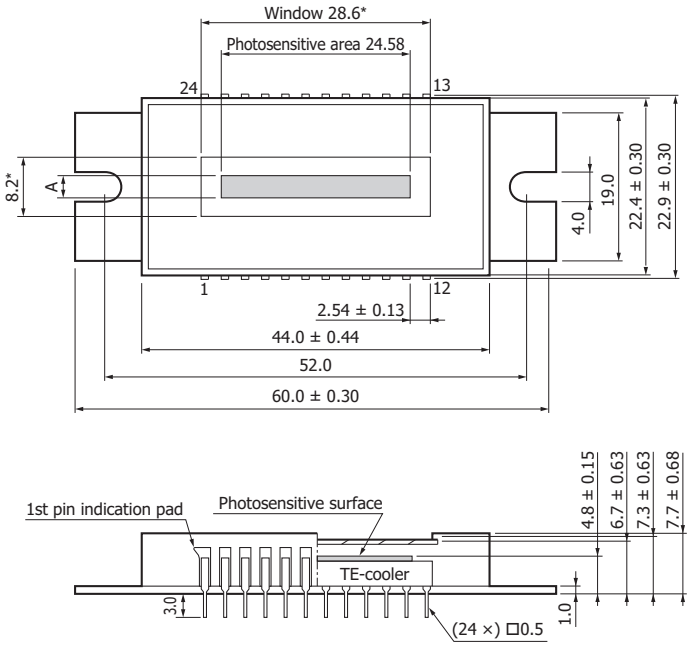
S10141-1107S/-1108S/-1109S



S10141-1107S: A=1.464
S10141-1108S: A=3.000
S10141-1109S: A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph.

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Pin connections

Pin no.	S10140 series		S10141 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	R_L=100 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+24 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*18	Transfer gate	TG*18	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

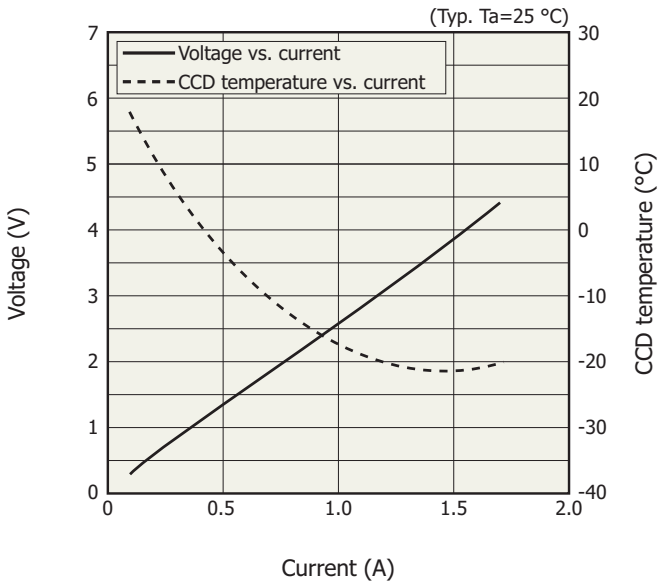
*18: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (Typ.)

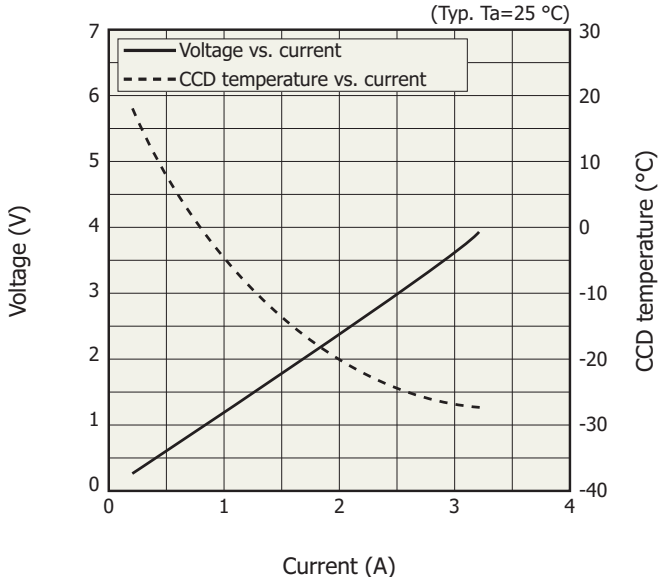
Parameter	Symbol	Condition	S10141-1007S/-1008S/-1009S	S10141-1107S/-1108S/-1109S	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current*19	Imax	Tc*20=Th*21=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc*20=Th*21=25 °C	3.8	3.6	V
Maximum heat absorption*21	Qmax		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

*19: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*20: Temperature of the cooling side of thermoelectric cooler.
*21: Temperature of the heat radiating side of thermoelectric cooler.
*22: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S10141-1007S/-1008S/-1009S



S10141-1107S/-1108S/-1109S

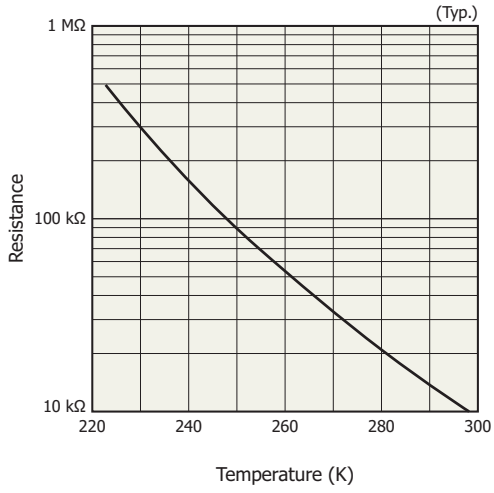


Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

RT1 = RT2 × exp BT1/T2 (1/T1 - 1/T2)
RT1: resistance at absolute temperature T1 [K]
RT2: Resistance at absolute temperature T2 [K]
BT1/T2: B constant [K]

The characteristics of the thermistor used are as follows.
R298=10 kΩ
B298/323=3450 K



Precautions (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

Related information

■ Precautions
http://jp.hamamatsu.com/sp/ssd/tech_pre_en.html

- Precautions for use (Image sensors)

Multichannel detector heads C10150, C10151

Features

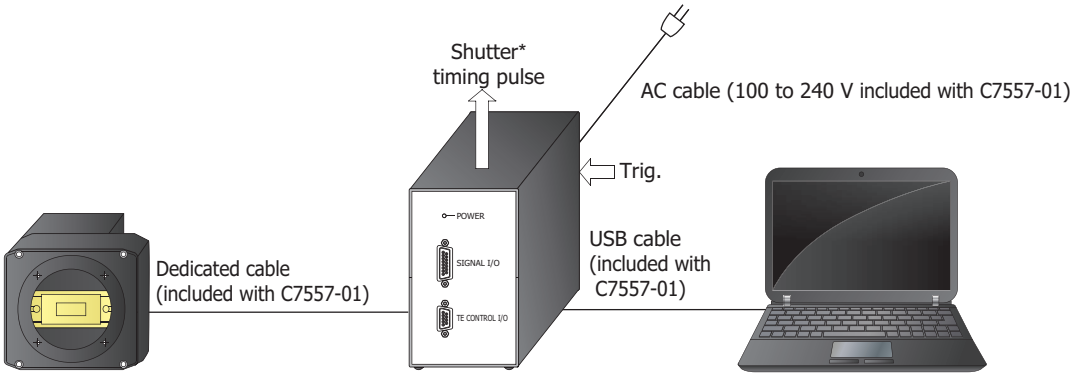
- **Designed for back-thinned CCD area image sensor**
  C10150: for non-cooled type (S10140 series)
  C10151: for TE-cooled type (S10141 series)
- **Line binning operation/area scanning operation**
- **Driver/amplifier circuit for low noise CCD operation**
- **Highly stable temperature controller (C10151)**
  Cooling temperature: -10 ± 0.05 °C
- **Simple signal input operation**
- **Compact configuration**

Multichannel detector head controller C7557-01

Features

- **For control of multichannel detector head and data acquisition**
- **Easy control and data acquisition using supplied software via USB interface**

Connection example



* Shutter, etc. are not available.

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