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CCD linear image sensor

S11490

High sensitivity in near infrared region, high-speed line rate

The S11490 is a back-thinned CCD linear image sensor designed via our advanced technology to deliver high sensitivity in the near infrared region. It also offers high-speed line rates of up to 30 kHz by multiport readout (10 MHz max. per port).

Features

- **High sensitivity in near infrared region: QE=70% (λ=900 nm), QE=40% (λ=1000 nm)**
- **High-speed line rate: 30 kHz max.**
- **Low etaloning**

Applications

- **OCT (optical coherence tomography)**
- **Spectrophotometry**

Structure

Parameter	Specification
Image size (H × V)	24.576 × 0.500 mm
Pixel size (H × V)	24 × 500 µm
Number of total pixels (H × V)	1056 × 1
Number of effective pixels (H × V)	1024 × 1
Horizontal clock phase	2 phases
Output circuit	Two-stage MOSFET source follower
Package	54-pin ceramic DIP (refer to dimensional outline)
Window	Borosilicate glass*1
Cooling	Non-cooled

*1: Resin sealing

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2 *3		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage		V_{OD}	-0.5	-	+25	V
Reset drain voltage		V_{RD}	-0.5	-	+18	V
Output amplifier return voltage		Vret	-0.5	-	+18	V
All reset drain voltage		V_{ARD}	-0.5	-	+18	V
Horizontal input source voltage		V_{ISH}	-0.5	-	+18	V
All reset gate voltage		V_{ARG}	-10	-	+15	V
Storage gate voltage		V_{STG}	-10	-	+15	V
Horizontal input gate voltage		V_{IG1H}, V_{IG2H}	-10	-	+15	V
Summing gate voltage		V_{SG}	-10	-	+15	V
Output gate voltage		V_{OG}	-10	-	+15	V
Reset gate voltage		V_{RG}	-10	-	+15	V
Transfer gate voltage		V_{TG}	-10	-	+15	V
Resistive gate voltage	High	V_{REGH}	-10	-	+15	V
	Low	V_{REGL}				
Horizontal shift register clock voltage		V_{P1H}, V_{P2H}	-10	-	+15	V

*2: Package temperature

*3: The sensor temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed. For more details, refer to the technical information "Resistive gate type CCD linear image sensors with electronic shutter".

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	15	18	V
Reset drain voltage			V_{RD}	14	15	16	V
Output amplifier return voltage*4			Vret	-	1	2	V
All reset drain voltage			V_{ARD}	11	12	13	V
Test point	Horizontal input source		V_{ISH}	-	V_{RD}	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	
All reset gate voltage		Low	V_{ARGL}	-6.5	-6	-5.5	V
Storage gate voltage*5			V_{STG1}	-1	0	0	V
			V_{STG2}	-1	0	1	V
Summing gate voltage		High	V_{SGH}	5	6	7	V
		Low	V_{SGL}	-6	-5	-4	
Output gate voltage			V_{OG}	4.5	5	5.5	V
Reset gate voltage		High	V_{RGH}	7	8	9	V
		Low	V_{RGL}	-6	-5	-4	
Transfer gate voltage		High	V_{TGH}	8	9	10	V
		Low	V_{TGL}	-8	-7	-6	
Resistive gate high voltage			V_{REGH}	-4	-3	-2	V
Resistive gate low voltage			V_{REGL}	-	V_{REGH} - 2.5	-	V
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	5	6	7	V
		Low	V_{P1HL}, V_{P2HL}	-6	-5	-4	
Substrate voltage			V_{SS}	-	0	-	V
External load resistance			R_L	2.0	2.2	2.4	kΩ

*4: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

*5: Set V_{STG1} lower than V_{STG2}.

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	5	10	MHz
Line rate	LR	-	10	30	kHz
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	200	-	pF
All reset gate capacitance	C_{ARG}	-	300	-	pF
Resistive gate capacitance	C_{REG}	-	1000	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Transfer gate capacitance	C_{TG}	-	300	-	pF
Charge transfer efficiency*6	CTE	0.99995	0.99999	-	-
DC output level	Vout	9	10	11	V
Output impedance	Zo	-	300	-	Ω
Output amplifier return current	Iret	-	0.4	-	mA
Power consumption	P_{AMP}*7	-	75	-	mW
	P_{REG}*8	0.6	3.1	6.3	
Resistive gate resistance*9	R_{REG}	0.5	1.5	5	kΩ

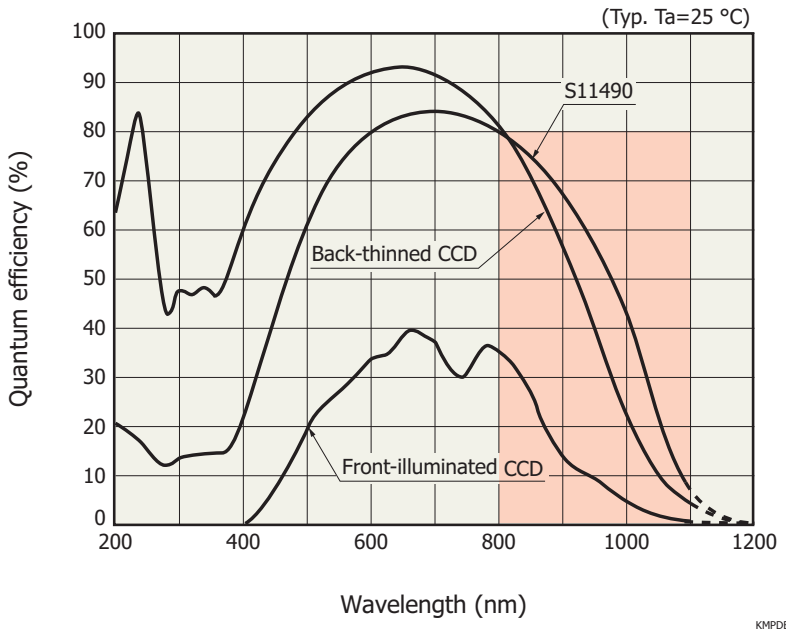
*6: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity
*7: Power consumption of the on-chip amplifier plus load resistance
*8: Power consumption at REG
*9: Resistance value between REGH and REGL

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted, operating condition: Typ.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Fw	400	500	-	ke^-
CCD node sensitivity	Sv	4	5	6	$\mu V/e^-$
Dark current (Non-MPP mode)*10	DS	-	120	600	ke^-/pixel/s
		-	80	400	pA/cm^2
Readout noise*11	Nr	-	100	150	e^- rms
Dynamic range*12	DR	2600	5000	-	-
Spectral response range	λ	-	320 to 1100	-	nm
Photoresponse nonuniformity*13 *14	PRNU	-	±3	±10	%
Image lag*13 *15	L	-	10	20	%

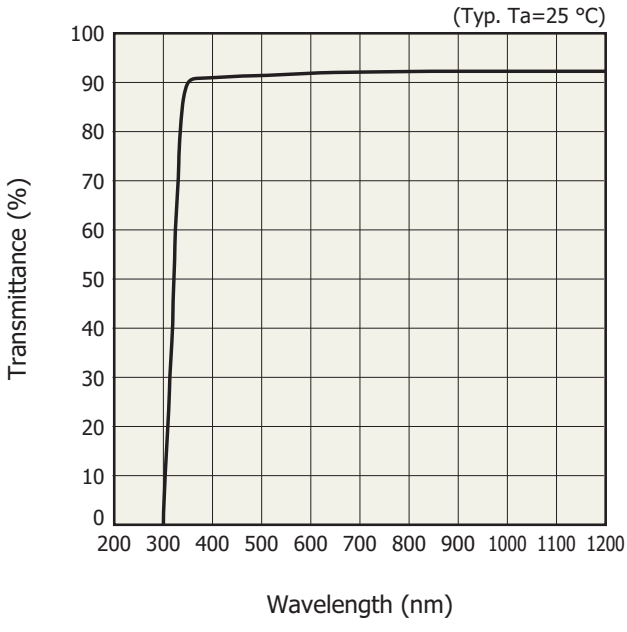
*10: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*11: Signal outoput frequency=30 MHz
*12: Dynamic range=Full well capacity/Readout noise
*13: Measured at one-half of the saturation output (full well capacity), using LED light (peak emission wavelength: 660 nm)
*14: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]
*15: The ratio of remaining signal after the image sensor is illuminated with one shot of pulsed light that produces one-half of the saturation output. For more details refer to our technical information on "Resistive gate type CCD linear image sensors with electronic shutter."

Spectral response (without window)*16

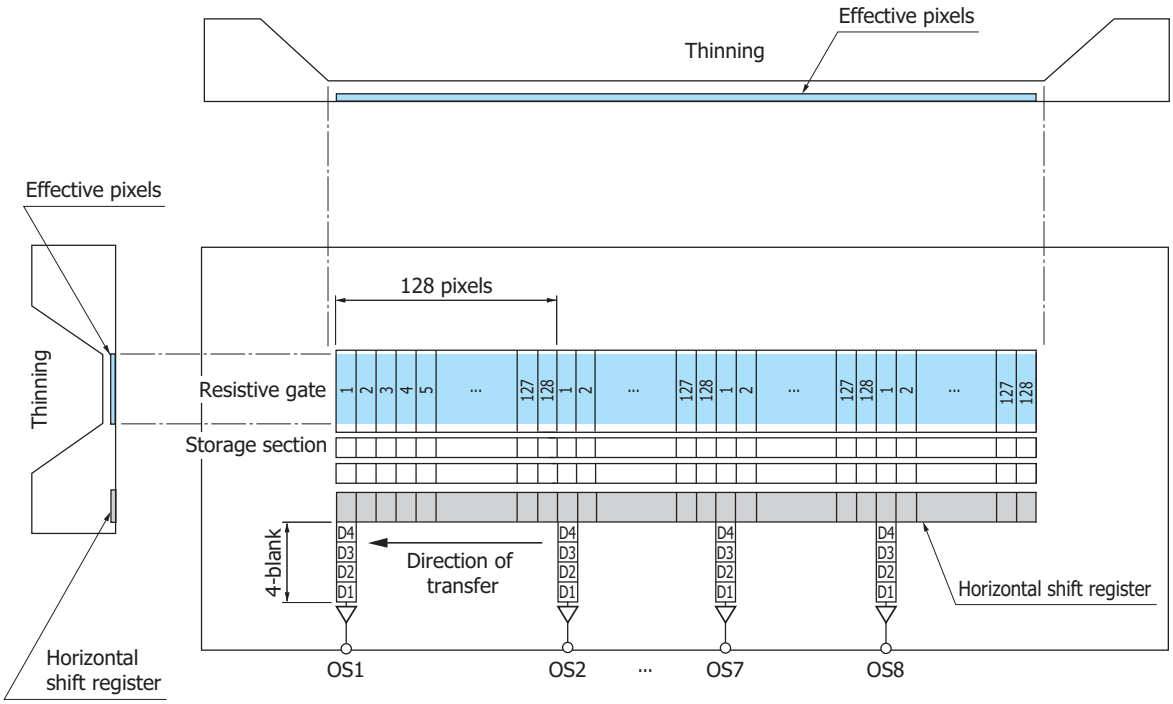


*16: Spectral response with borosilicate glass is decreased according to the spectral transmittance characteristics of window material.

Spectral transmittance characteristics of window material



Device structure (conceptual drawing of top view in dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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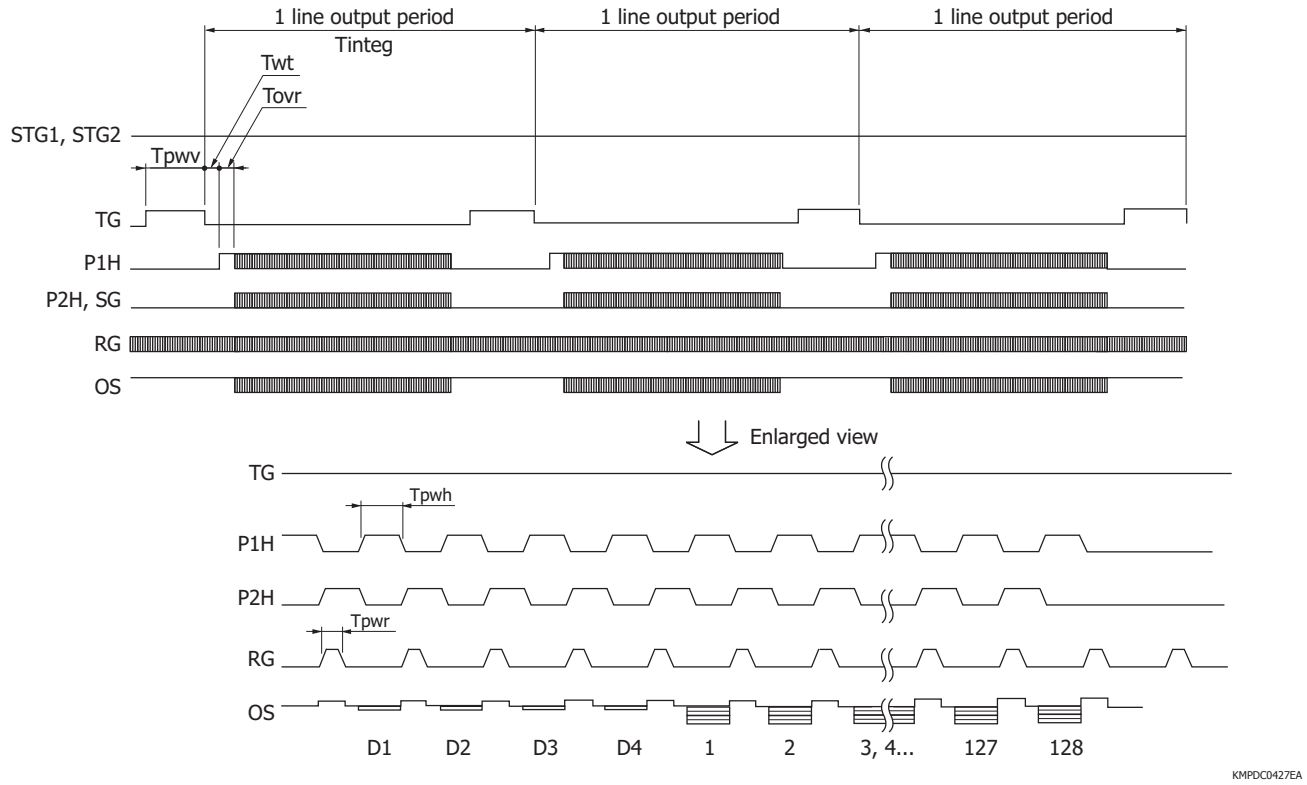
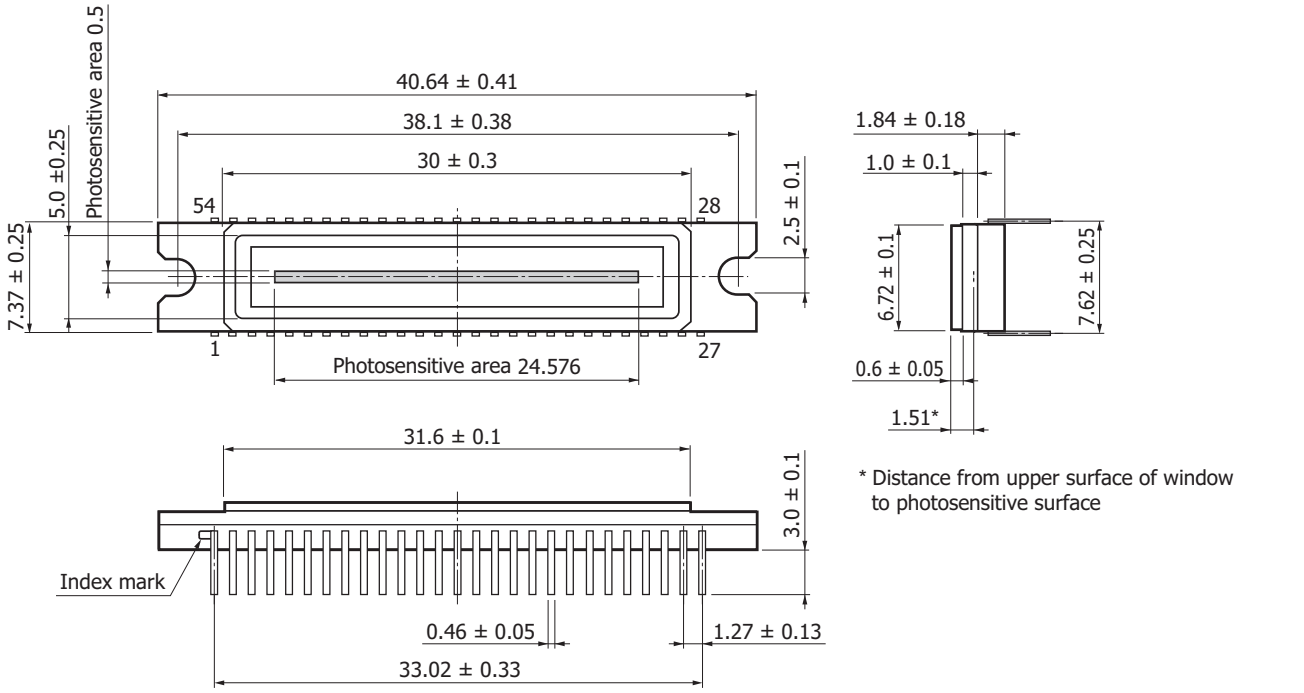
Timing chart



Parameter		Symbol	Min.	Typ.	Max.	Unit
TG	Pulse width	Tpwv	0.6	1.2	-	µs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*17	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	200	400	-	ns
	Standby time	Twt	-	15	-	ns
Integration time		Tinteg	33	66	-	µs

*17: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



* Distance from upper surface of window to photosensitive surface

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Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	Vret	Output amplifier return	+1 V
2	OG	Output gate	+5 V
3	RD	Reset drain	+15 V
4	Vret	Output amplifier return	+1 V
5	OS1	Output transistor source 1	R_L=2.2 kΩ
6	OD1	Output transistor drain 1	+15 V
7	OS2	Output transistor source 2	R_L=2.2 kΩ
8	OD2	Output transistor drain 2	+15 V
9	Vret	Output amplifier return	+1 V
10	OS3	Output transistor source 3	R_L=2.2 kΩ
11	OD3	Output transistor drain 3	+15 V
12	OS4	Output transistor source 4	R_L=2.2 kΩ
13	OD4	Output transistor drain 4	+15 V
14	Vret	Output amplifier return	+1 V
15	OS5	Output transistor source 5	R_L=2.2 kΩ
16	OD5	Output transistor drain 5	+15 V
17	OS6	Output transistor source 6	R_L=2.2 kΩ
18	OD6	Output transistor drain 6	+15 V
19	Vret	Output amplifier return	+1 V
20	OS7	Output transistor source 7	R_L=2.2 kΩ
21	OD7	Output transistor drain 7	+15 V
22	OS8	Output transistor source 8	R_L=2.2 kΩ
23	OD8	Output transistor drain 8	+15 V
24	Vret	Output amplifier return	+1 V
25	IGH	Test point (horizontal input gate)	-8 V
26	ISH	Test point (horizontal input source)	Connect to RD
27	Vret	Output amplifier return	+1 V
28	SS	Substrate	GND
29	TG	Transfer gate	
30	STG2	Storage gate 2	0 V
31	REGH	Resistive gate (High)	-3 V
32	STG1	Storage gate 1	0 V
33	SS	Substrate	GND
34	ARD	All reset drain	+12 V
35	ARG	All reset gate	
36	REGL	Resistive gate (Low)	-5.5 V
37	SS	Substrate	GND
38	SG	Summing gate	
39	SS	Substrate	GND
40	P1H	CCD horizontal shift register clock-1	
41	SS	Substrate	GND
42	P2H	CCD horizontal shift register clock-2	
43	SS	Substrate	GND
44	RG	Reset gate	
45	SS	Substrate	GND
46	REGL	Resistive gate (Low)	-5.5 V
47	ARG	All reset gate	
48	ARD	All reset drain	+12 V
49	SS	Substrate	GND
50	STG1	Storage gate 1	0 V
51	REGH	Resistive gate (High)	-3 V
52	STG2	Storage gate 2	0 V
53	TG	Transfer gate	
54	SS	Substrate	GND

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical information
· Resistive gate type CCD linear image sensors with electronic shutter

HAMAMATSU www.hamamatsu.com

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 8152-375-0, Fax: (49) 8152-265-8
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39) 02-93581733, Fax: (39) 02-93581741
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, Beijing 100020, China, Telephone: (86) 10-6586-6006, Fax: (86) 10-6586-2866

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