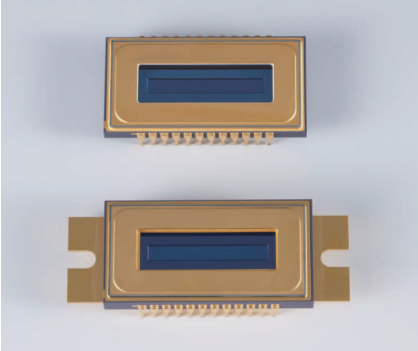
HAMAMATSU
PHOTON IS OUR BUSINESS

IR-enhanced CCD area image sensors



S11500-1007, S11501-1007S

Enhanced near infrared sensitivity: QE=40% (λ=1000 nm), back-thinned FFT-CCD

The S11500-1007 and S11501-1007S are FFT-CCD image sensors for photometric applications that offers improved sensitivity in the near infrared region at wavelengths longer than 800 nm. Our unique technology in laser processing was used to form a MEMS structure on the back side of the CCD. This allows the S11500-1007 and S11501-1007S to have much higher sensitivity than our previous products (S7030/S7031 series).
In addition to having high near infrared sensitivity, the S11500-1007 and S11501-1007S can be used as an image sensor with a long photosensitive area in the direction of the sensor height by binning operation, making it suitable for detectors in Raman spectroscopy. Binning operation also ensures even higher S/N and signal processing speed compared to methods that use an external circuit to add signals digitally.
The S11500-1007 and S11501-1007S have a pixel size of 24 × 24 µm and image size of 24.576 (H) × 2.928 (V) mm (1024 × 122 pixels). The S11500-1007 and S11501-1007S are pin compatible with the S7030/S7031 series, and so operate under the same drive conditions.

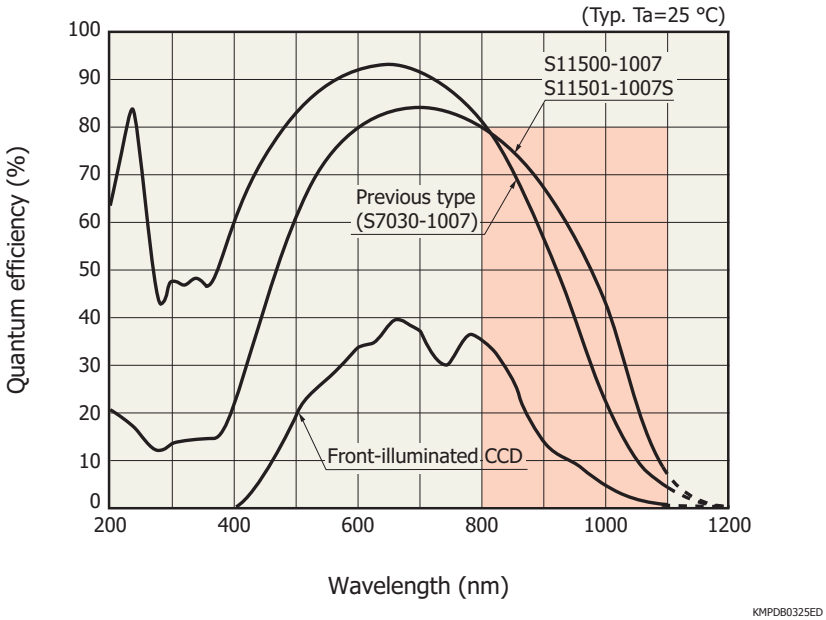
Features

- **Enhanced near infrared sensitivity: QE=40% (λ=1000 nm)**
- **Pixel size: 24 × 24 µm**
- **Line, pixel binning**
- **Wide spectral response range**
- **Low readout noise**
- **Wide dynamic range**
- **MPP operation**

Applications

- **Raman spectrometer, etc.**

Spectral response (without window)*1



*1: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

Structure

Parameter	S11500-1007	S11501-1007S
Pixel size (H × V)	24 × 24 µm	
Number of total pixels (H × V)	1044 × 128	
Number of effective pixels (H × V)	1024 × 122	
Image size (H × V)	24.576 × 2.928 mm	
Vertical clock phase	2-phase	
Horizontal clock phase	2-phase	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outline)	
Window	Quartz glass*2	AR coated sapphire
Cooling	Non-cooled	One-stage TE-cooled

*2: Resin sealing

Absolute maximum ratings

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*3		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage		V_{OD}	-0.5	-	+25	V
Reset drain voltage		V_{RD}	-0.5	-	+18	V
Vertical input source voltage		V_{ISV}	-0.5	-	+18	V
Horizontal input source voltage		V_{ISH}	-0.5	-	+18	V
Vertical input gate voltage		V_{IG1V}, V_{IG2V}	-10	-	+15	V
Horizontal input gate voltage		V_{IG1H}, V_{IG2H}	-10	-	+15	V
Summing gate voltage		V_{SG}	-10	-	+15	V
Output gate voltage		V_{OG}	-10	-	+15	V
Reset gate voltage		V_{RG}	-10	-	+15	V
Transfer gate voltage		V_{TG}	-10	-	+15	V
Vertical shift register clock voltage		V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal shift register clock voltage		V_{P1H}, V_{P2H}	-10	-	+15	V
TE-cooler maximum current*4	Tc*5=Th*6=25 °C	Imax	-	-	3.0	A
TE-cooler maximum voltage	Tc*5=Th*6=25 °C	Vmax	-	-	3.6	V
Maximum temperature of heat radiating side		-	-	-	70	°C

*3: Package temperature
*4: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*5: Temperature of the cooling side of thermoelectric cooler
*6: Temperature of the heat radiating side of thermoelectric cooler
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	18	20	22	V
Reset drain voltage			V_{RD}	11.5	12	12.5	V
Output gate voltage			V_{OG}	1	3	5	V
Substrate voltage			V_{SS}	-	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Horizontal input source		V_{ISH}	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	V
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	4	6	8	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	4	6	8	V
		Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	4	6	8	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	4	6	8	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	
External load resistance			R_L	20	22	24	kΩ

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	0.25	1	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}		3000	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	180	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Transfer gate capacitance	C_{TG}	-	75	-	pF
Charge transfer efficiency*7	CTE	0.99995	0.99999	-	-
DC output level	Vout	14	16	18	V
Output impedance	Zo	-	3	4	kΩ
Power consumption*8	P	-	13	14	mW

*7: Charge transfer efficiency per pixel, measured at half of the full well capacity
*8: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

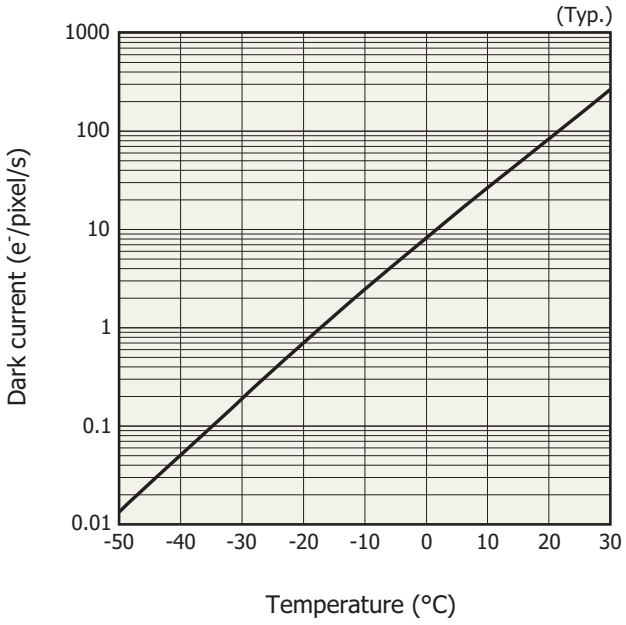
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical		Fw	240	320	-	ke⁻
	Horizontal*9			800	1000	-	
CCD node sensitivity			Sv	1.8	2.2	-	μV/e⁻
Dark current*10 (MPP mode)	25 °C		DS	-	100	400	e⁻/pixel/s
	0 °C			-	10	40	
Readout noise*11			Nr	-	8	16	e⁻ rms
Dynamic range*12	Line binning		DR	100000	125000	-	-
	Area scanning			30000	40000	-	-
Photoresponse nonuniformity*13			PRNU	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*14	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect*15			-	-	3	-
	Column defect*16			-	-	0	-

*9: The linearity is ±1.5 %.
*10: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*11: Measured with a HAMAMATSU C4880 digital CCD camera with a CDS circuit (sensor temperature: -40 °C, operating frequency: 150 kHz)
*12: Dynamic range = Full well capacity / Readout noise
*13: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

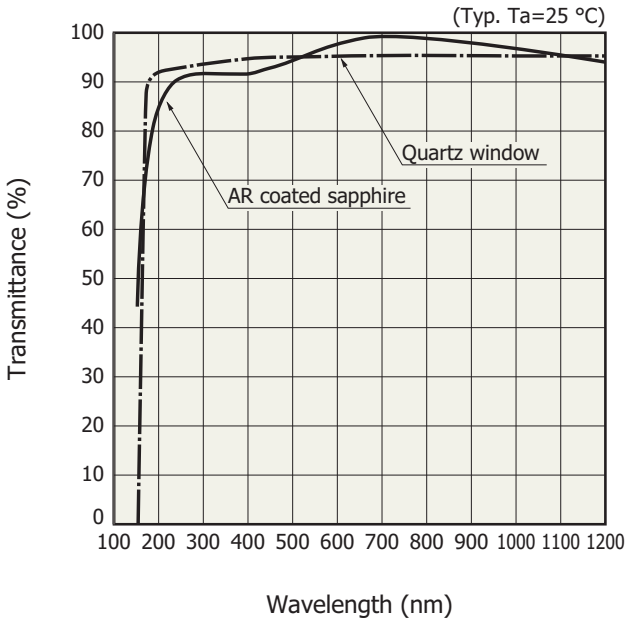
*14: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at 0 °C.
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output. (measured with uniform light producing one-half of the saturation charge)
*15: 2 to 9 contiguous defective pixels
*16: 10 or more contiguous defective pixels

Dark current vs. temperature



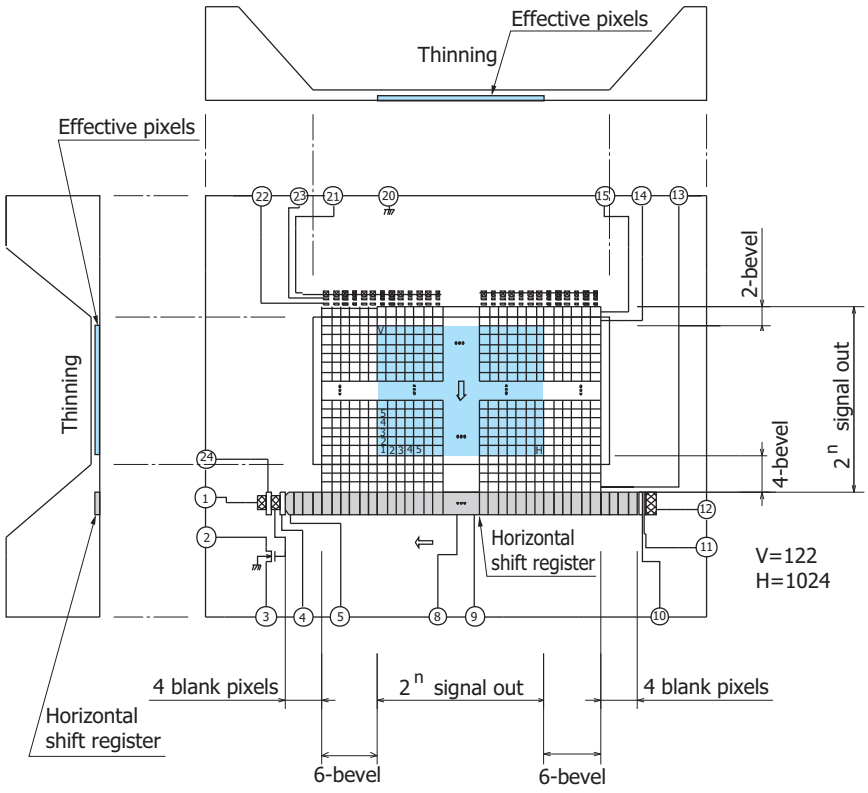
KMPDB0256EA

Spectral transmittance characteristics



KMPDB0110EA

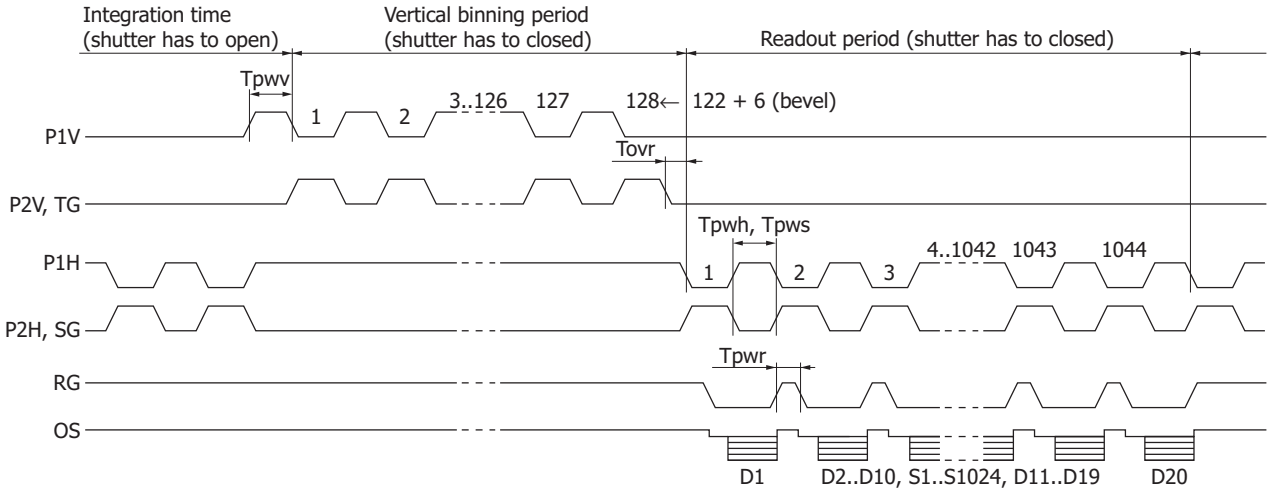
Device structure (conceptual drawing of top view)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPDC0364EB

Timing chart (line binning)

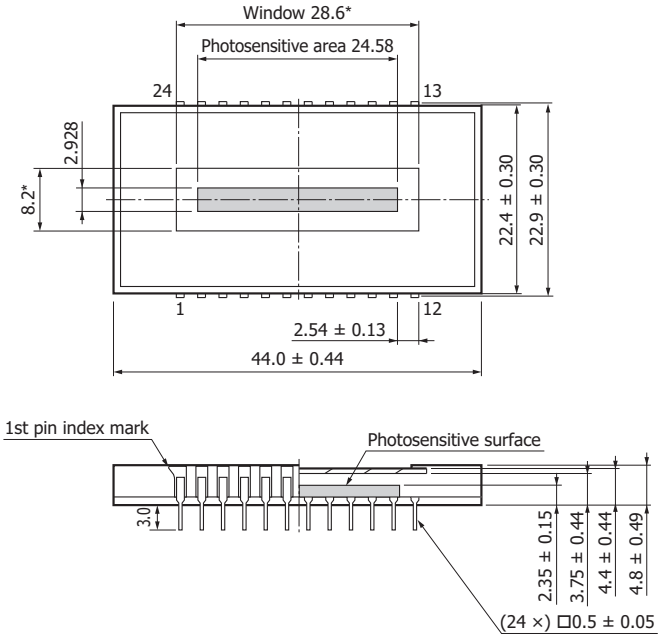


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG*17	Pulse width	Tpwv	6	8	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H*17	Pulse width	Tpwh	500	2000	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	500	2000	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	100	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG-P1H	Overlap time	Tovr	3	-	-	µs

*17: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

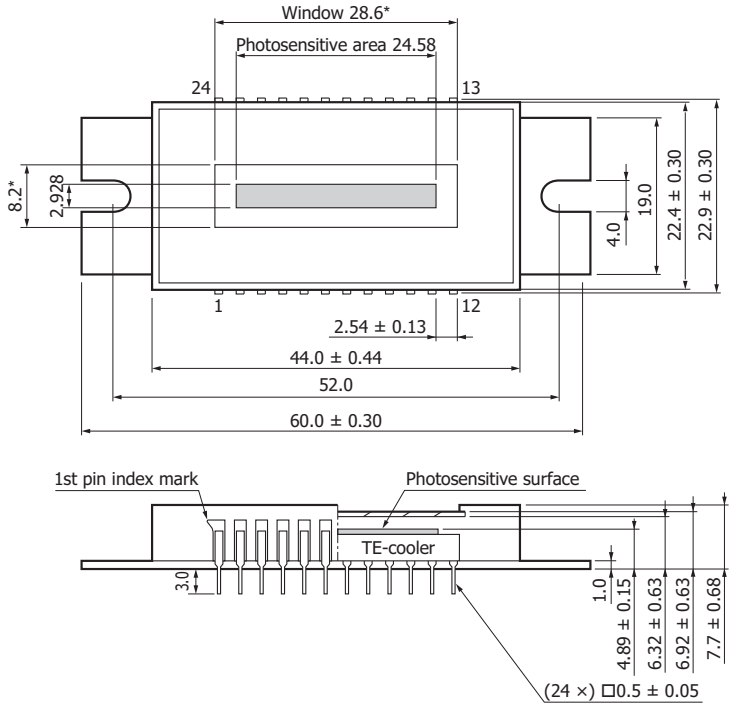
S11500-1007



* Area of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

KMPDA0264EB

S11501-1007S



* Area of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph

KMPDA0328EA

Pin connections

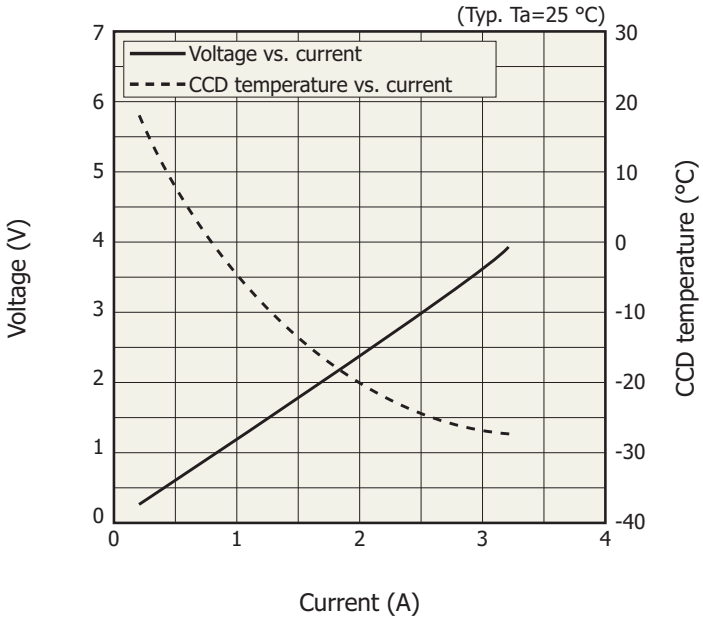
Pin no.	S11500-1007		S11501-1007S		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	R_L=22 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*18	Transfer gate	TG*18	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-8 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-8 V
24	RG	Reset gate	RG	Reset gate	

*18: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (S11501-1007S, Typ.)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	1.2	Ω
Maximum heat absorption*19	Qmax		5.1	W

*19: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



KMPDB0179EA

Specifications of built-in temperature sensor (S11501-1007S)

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: Resistance at absolute temperature T1 [K]

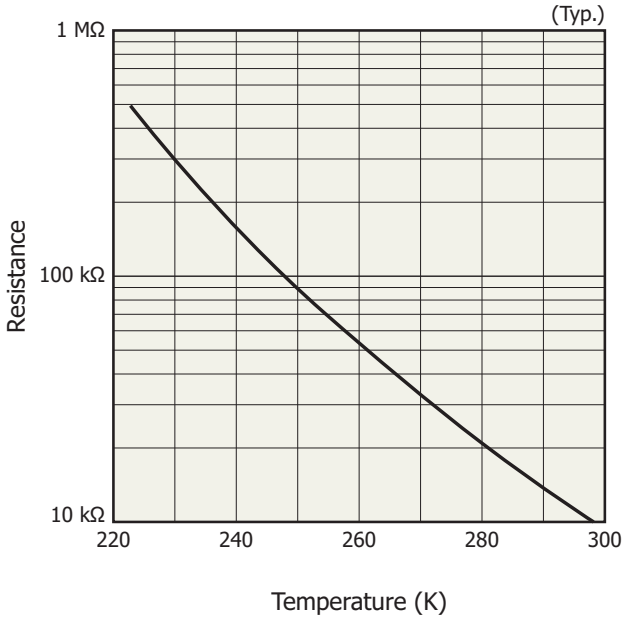
R_{T2}: Resistance at absolute temperature T2 [K]

$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.

R_{298}=10 kΩ

$B_{298/323}$=3450 K



KMPDB0111EB

Precautions (electrostatic countermeasures)

· When handling CCD sensors, always wear a wrist strap and also anti-static clothing, gloves, and shoes, etc. The wrist strap should have a protective resistor (about 1 MΩ) on the side closer to the body and be grounded properly. Using a wrist strap having no protective resistor is hazardous because you may receive an electrical shock if electric leakage occurs.
· Avoid directly placing these sensors on a work bench that may carry an electrostatic charge.
· Provide ground lines with the work bench and work floor to allow static electricity to discharge.
· Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors

■ Technical information

· FFT-CCD area image sensor

Multichannel detector heads C7040, C7041

Features

- **C7040: for S7030 series and S11500-1007**
  C7041: for S7031 series and S11501-1007S
- **Area scanning or full line-binnng operation**
- **Readout frequency: 250 kHz**
- **Readout noise: 20 e^- rms**
- **ΔT=50 °C (ΔT changes by cooling method.)**

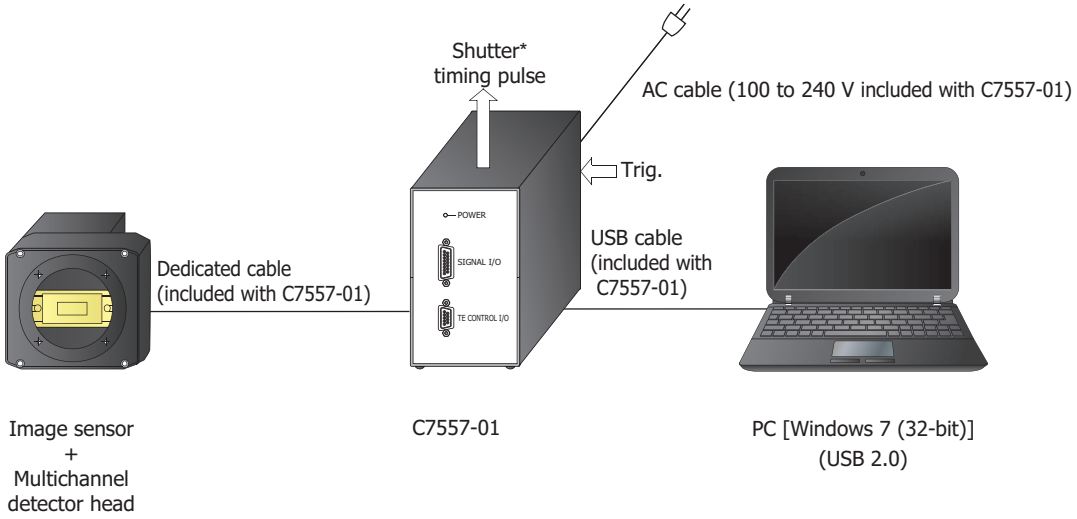
Input	Symbol	Specification
Supply voltage	V_{D1}	+5 Vdc, 200 mA
	V_{A1+}	+15 Vdc, +100 mA
	V_{A1-}	-15 Vdc, -100 mA
	V_{A2}	+24 Vdc, 30 mA
	V_{D2}	+5 Vdc, 30 mA (C7041)
	Vp	+5 Vdc, 2.5 A (C7041)
	V_F	+12 Vdc, 100 mA (C7041)
Master start	ϕms	HCMOS logic compatible
Master clock	ϕmc	HCMOS logic compatible, 1 MHz

Multichannel detector head controller C7557-01

Features

- **For control of multichannel detector head and data acquisition**
- **Easy control and data acquisition using supplied software via USB interface**

Connection example



* Shutter, etc. are not available.

KACCC0402EC

Information described in this material is current as of December, 2015.
Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.
The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use.
Copying or reprinting the contents described in this material in whole or in part is prohibited without our prior permission.

HAMAMATSU www.hamamatsu.com

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 8152-375-0, Fax: (49) 8152-265-8
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39) 02-93581733, Fax: (39) 02-93581741
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, Beijing 100020, China, Telephone: (86) 10-6586-6006, Fax: (86) 10-6586-2866

Cat. No. KMPD1125E06 Dec. 2015 DN