

## S11511 series

### Enhanced near infrared sensitivity, Constant element temperature control

The S11511 series is a family of FFT (full frame transfer)-CCD image sensors for photometric applications that offer improved sensitivity in the near infrared region at wavelengths longer than 800 nm. Our unique technology in laser processing was used to form a MEMS structure on the back side of the CCD. This allows the S11510 series to have much higher sensitivity than our previous products (S11850 series).

In addition to having high infrared sensitivity, the S11510 series can be used as an image sensor with a long active area in the direction of the sensor height by binning operation, making it suitable for detectors in Raman spectroscopy. Binning operation also ensures even higher S/N and signal processing speed compared to methods that use an external circuit to add signals digitally. In addition, a TE-cooler is built into the package to keep the element temperature constant (approx. 5 °C) during operation.

The S11511 series has a pixel size of 14 × 14 μm and is available in two image areas of 14.336 (H) × 0.896 (V) mm (1024 × 64 pixels) and 28.672 (H) × 0.896 (V) mm (2048 × 64 pixels). The S11511 series is pin compatible with the S11850-1106, and so operates under the same drive conditions.

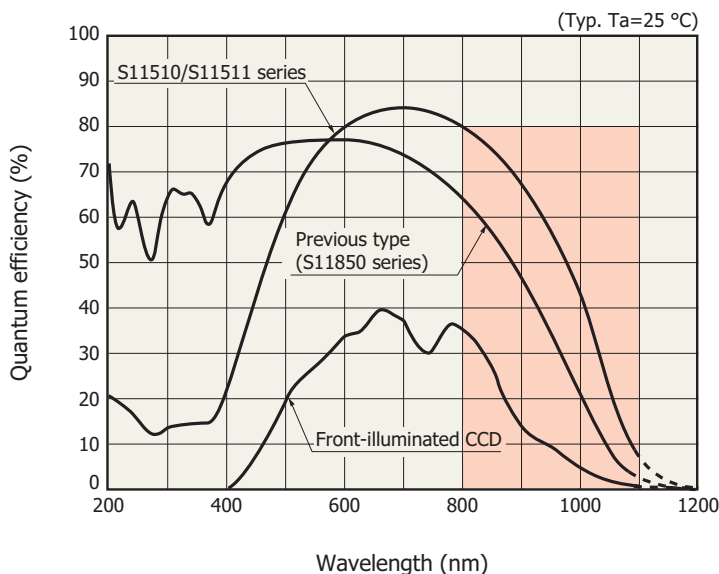
#### Features

- NIR high sensitivity: QE=40% (λ=1000 nm)
- One-stage TE-cooled type (element temperature: approx. 5 °C)
- High CCD node sensitivity: 6.5 μV/e<sup>-</sup>
- High full well capacity, wide dynamic range (with anti-blooming function)
- Pixel size: 14 × 14 μm
- MPP operation

#### Applications

- Raman spectrometers, etc.

#### Spectral response (without window)\*1



\*1: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

**Structure**

Parameter	S11511-1006	S11511-1106	Unit
Image size (H × V)	14.336 × 0.896	28.672 × 0.896	mm
Pixel size (H × V)	14 × 14		μm
Number of total pixels	1044 × 70	2068 × 70	-
Number of effective pixels	1024 × 64	2048 × 64	-
Vertical clock phase	2-phase		-
Horizontal clock phase	4-phase		-
Output circuit	One-stage MOSFET source follower		-
Package	28-pin ceramic DIP (refer to dimensional outline)		-
Window	Quartz glass*2		-

\*2: Hermetic sealing

**Absolute maximum ratings (Ta=25 °C, unless otherwise noted)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature*3	Topr		-50	-	+50	°C
Storage temperature	Tstg		-50	-	+70	°C
Output transistor drain voltage	VOD		-0.5	-	+30	V
Reset drain voltage	VRD		-0.5	-	+18	V
Overflow drain voltage	VOFD		-0.5	-	+18	V
Vertical input source voltage	VISV		-0.5	-	+18	V
Horizontal input source voltage	VISH		-0.5	-	+18	V
Overflow gate voltage	VOFG		-10	-	+15	V
Vertical input gate voltage	VIG1V, VIG2V		-10	-	+15	V
Horizontal input gate voltage	VIG1H, VIG2H		-10	-	+15	V
Summing gate voltage	VSG		-10	-	+15	V
Output gate voltage	VOG		-10	-	+15	V
Reset gate voltage	VRG		-10	-	+15	V
Transfer gate voltage	VTG		-10	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V		-10	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H VP3H, VP4H		-10	-	+15	V
TE-cooler maximum current*4 *5	Imax	Tc*6=Th*7=25 °C	-	1.8	-	A
TE-cooler maximum voltage	Vmax	Tc*6=Th*7=25 °C	-	3.5	-	V
Thermistor power dissipation	Pd_th		-	-	100	mW

\*3: Chip temperature

\*4: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.

\*5: To ensure stable temperature control, ΔT (temperature difference between Th and Tc) should be less than 30 °C. If ΔT exceeds 30 °C, product characteristics may deteriorate. For example, the dark current uniformity may degrade.

\*6: Temperature of the cooling side of thermoelectric cooler

\*7: Temperature of the heat radiating side of thermoelectric cooler

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	23	24	25	V	
Reset drain voltage	VRD	11	12	13	V	
Overflow drain voltage	VOFD	11	12	13	V	
Test point	Input source	VISV, VISH	-	VRD	-	V
	Vertical input gate	VIG1V, VIG2V	-9	-8	-	V
	Horizontal input gate	VIG1H, VIG2H	-9	-8	-	V
Overflow gate voltage	VOFG	0	12	13	V	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-6	-5	-4	
Output gate voltage	VOG	4	5	6	V	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-6	-5	-4	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH VP3HH, VP4HH	4	6	8	V
	Low	VP1HL, VP2HL VP3HL, VP4HL	-6	-5	-4	
Substrate voltage	VSS	-	0	-	V	
External load resistance	RL	90	100	110	kΩ	

▣ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Signal output frequency*8	fc	-	0.25	0.5	MHz	
Vertical shift register capacitance	-1006 -1106	CP1V, CP2V	-	600	-	pF
			1200			
Horizontal shift register capacitance	-1006 -1106	CP1H, CP2H CP3H, CP4H	-	80	-	pF
			160			
Summing gate capacitance	CSG	-	10	-	pF	
Reset gate capacitance	CRG	-	10	-	pF	
Transfer gate capacitance	-1006 -1106	CTG	-	30	-	pF
			60			
Charge transfer efficiency*9	CTE	0.99995	0.99999	-	-	
DC output level*8	Vout	17	18	19	V	
Output impedance*8	Zo	-	10	-	kΩ	
Power consumption*8 *10	P	-	4	-	mW	

\*8: The values depend on the load resistance. (VOD=24 V, RL=100 kΩ)

\*9: Charge transfer efficiency per pixel, measured at half of the full well capacity

\*10: Power consumption of the on-chip amplifier plus load resistance

**Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	50	60	-	ke <sup>-</sup>
	Horizontal	250	300	-	
CCD node sensitivity*11	Sv	5.5	6.5	7.5	μV/e <sup>-</sup>
Dark current*12	DS	-	50	500	e <sup>-</sup> /pixel/s
Readout noise*13	Nr	-	6	15	e <sup>-</sup> rms
Dynamic range*14	Line binning	DR	41700	50000	-
Spectral response range	λ	-	200 to 1100	-	nm
Photoresponse nonuniformity*15	PRNU	-	±3	±10	%

\*11: The values depend on the load resistance. (V<sub>OD</sub>=24 V, R<sub>L</sub>=100 kΩ)

\*12: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.

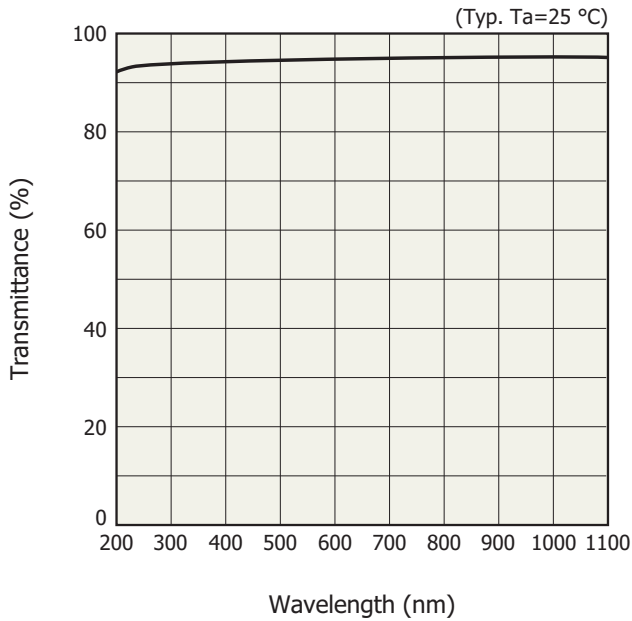
\*13: T<sub>d</sub>=-40 °C, f<sub>c</sub>=20 kHz

\*14: Dynamic range = Full well capacity / Readout noise

\*15: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

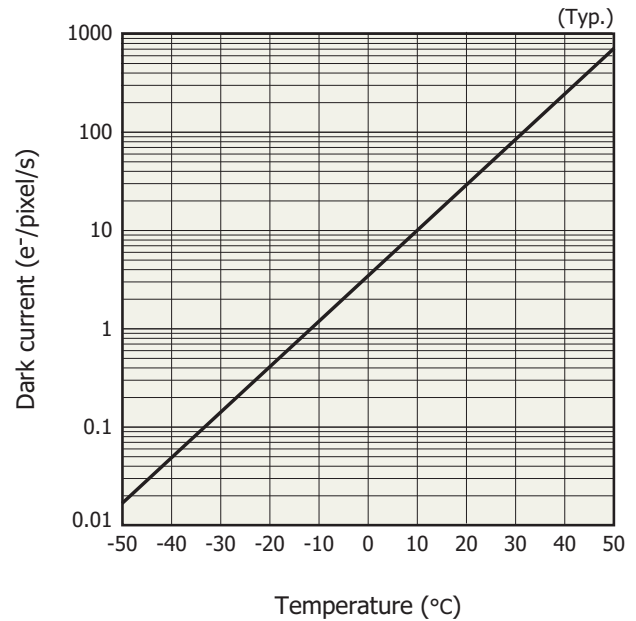
$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 [\%]$$

**Spectral transmittance characteristics of window material**



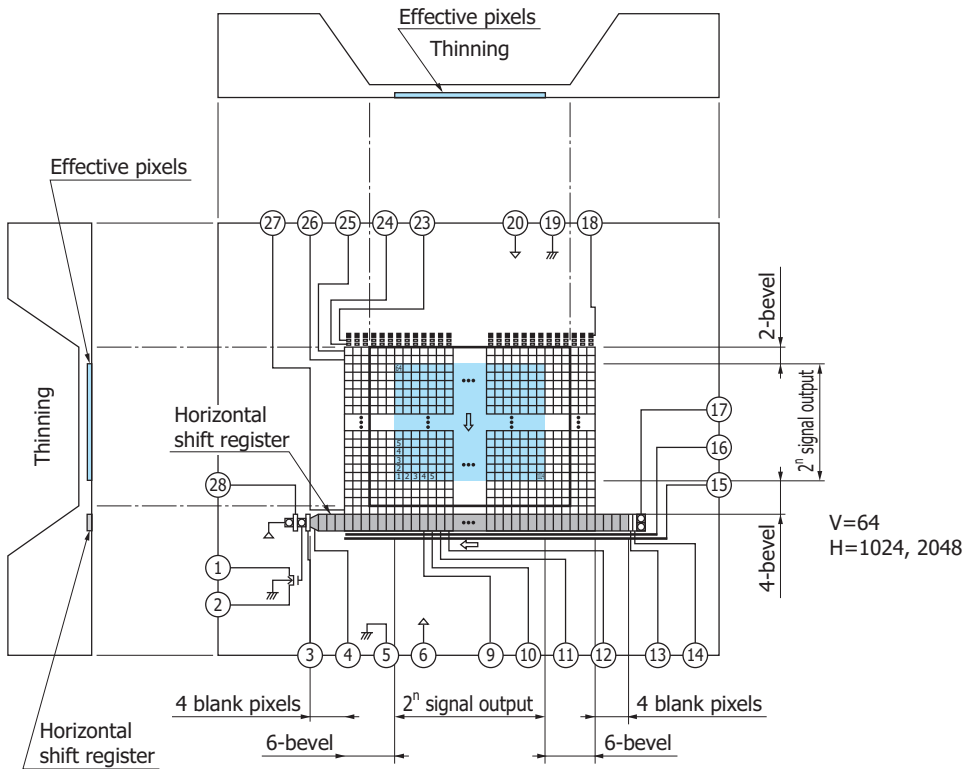
KMPD80303EB

**Dark current vs. temperature**



KMPD80304EB

Device structure (conceptual drawing of top view in dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPDC0596EA





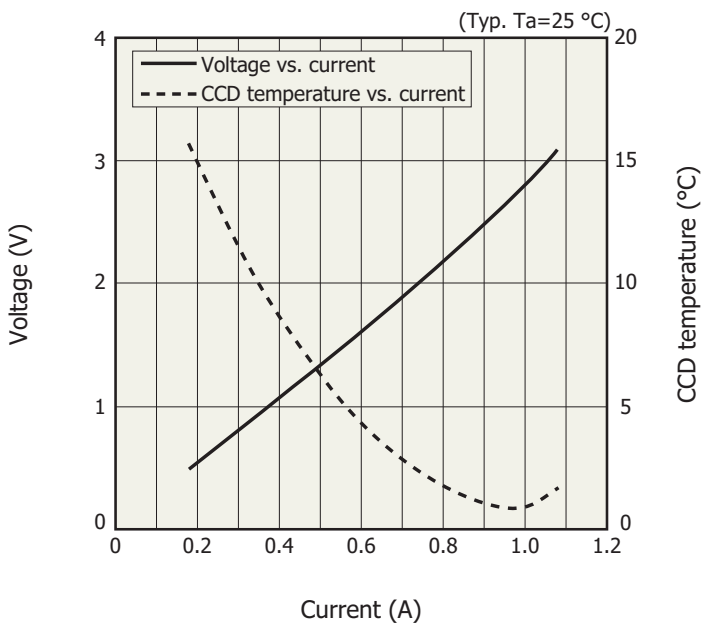
**Pin connections**

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	Th1	Thermistor	
8	P-	TE-cooler-	
9	P4H	CCD horizontal register clock-4	
10	P3H	CCD horizontal register clock-3	
11	P2H	CCD horizontal register clock-2	
12	P1H	CCD horizontal register clock-1	
13	IG2H	Test point (horizontal input gate-2)	-8 V
14	IG1H	Test point (horizontal input gate-1)	-8 V
15	OFG	Overflow gate	+12 V
16	OFD	Overflow drain	+12 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	ISV	Test point (vertical input source)	Connect to RD
19	SS	Substrate	GND
20	RD	Reset drain	+12 V
21	P+	TE-cooler+	
22	Th2	Thermistor	
23	IG2V	Test point (vertical input gate-2)	-8 V
24	IG1V	Test point (vertical input gate-1)	-8 V
25	P2V	CCD vertical register clock-2	
26	P1V	CCD vertical register clock-1	
27	TG	Transfer gate	Same pulse as P2V
28	RG	Reset gate	

**Specifications of built-in TE-cooler (Typ., vacuum condition)**

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	R <sub>int</sub>	T <sub>a</sub> =25 °C	1.6	Ω
Maximum heat absorption*17	Q <sub>max</sub>		4.0	W

\*17: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



KMPDB0469EA



**Specifications of built-in temperature sensor**

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$$

R<sub>T1</sub>: Resistance at absolute temperature T1 [K]

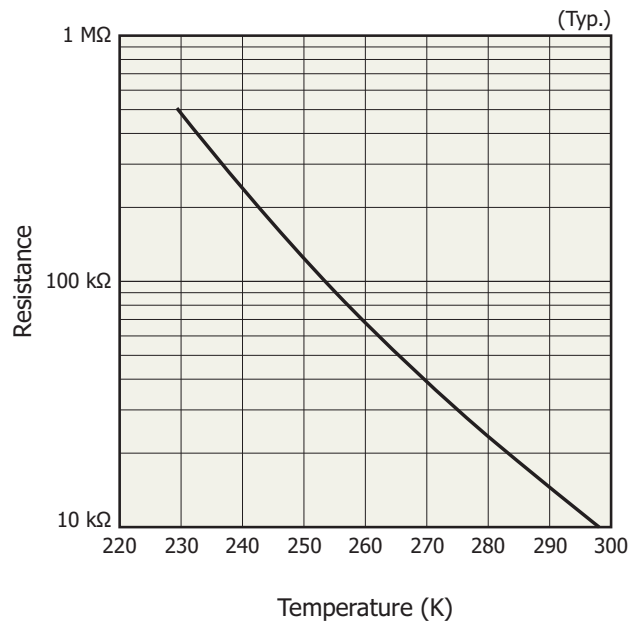
R<sub>T2</sub>: Resistance at absolute temperature T2 [K]

B<sub>T1/T2</sub>: B constant [K]

The characteristics of the thermistor used are as follows.

R<sub>298</sub>=10 kΩ

B<sub>298/323</sub>=3900 K



KMPD800470EA

**Precautions**

- If the thermoelectric cooler does not radiate away sufficient heat, then the product temperature will rise and cause physical damage or deterioration to the product. Make sure there is sufficient heat dissipation during cooling. As a heat dissipation measure, we recommend applying a high heat-conductivity material (silicone grease, etc.) over the entire area between the product and the heat-sink (metallic block, etc.), and screwing and securing the product to a heatsink.
- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

**Related information**

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

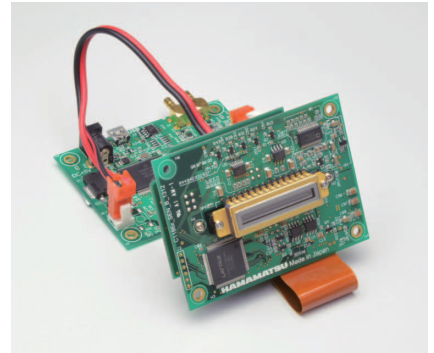
- Precautions
  - Disclaimer
  - Image sensors
- Technical information
  - FFT-CCD area image sensor

Driver circuit C11860 (sold separately) for CCD image sensor (S11850-1106, S11511 series)

The C11860 is a driver circuit developed for the Hamamatsu CCD image sensor S11850-1106 and S11511 series.

### Features

- **Built-in 16-bit A/D converter**
- **The sensor circuit board and interface circuit board are connected using a flexible cable.**
- **Interface: USB 2.0**
- **External synchronization capable**
- **Single power supply: +5 VDC**
- **Sensor cooling control (approx. +5 °C)**



Information described in this material is current as of October 2016.

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[www.hamamatsu.com](http://www.hamamatsu.com)

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 8152-375-0, Fax: (49) 8152-265-8

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39) 02-93581733, Fax: (39) 02-93581741

China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, Beijing 100020, China, Telephone: (86) 10-6586-6006, Fax: (86) 10-6586-2866