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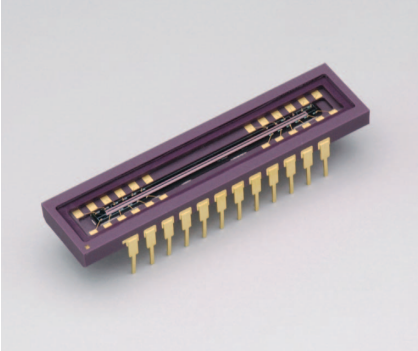
CCD linear image sensor



S12551-2048

Pixel size: 14 × 14 µm, front-illuminated type, high-speed response and high sensitivity

The S12551-2048 is a front-illuminated type CCD linear image sensor with high-speed line rate designed for applications such as sorting machine.

Features

- **Pixel size: 14 × 14 µm**
- **2048 pixels**
- **High CCD node sensitivity: 13 µV/e⁻ typ.**
- **Readout speed: 40 MHz max.**
- **Anti-blooming function**
- **Built-in electronic shutter**

Applications

- **Foreign object screening**
- **High-speed imaging**

Structure

Parameter	Specification
Pixel size (H × V)	14 × 14 µm
Number of pixels	2068
Number of effective pixels	2048
Image size (H × V)	28.672 × 0.014 mm
Horizontal clock phase	Two-phase
Output circuit	Three-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outline)
Window material	Quartz glass*1

*1: Resin sealing

Absolute maximum ratings (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Condition	Value	Unit
Operating temperature	Topr	Package temperature, No dew condensation*2	-50 to +60	°C
Storage temperature	Tstg	No dew condensation*2	-50 to +70	°C
Output transistor drain voltage	V_{OD}		-0.5 to +20	V
Reset drain voltage	V_{RD}		-0.5 to +18	V
Anti-blooming drain voltage	V_{ABD}		-0.5 to +18	V
Horizontal input source voltage	V_{ISH}		-0.5 to +18	V
Anti-blooming gate voltage	V_{ABG}		-10 to +15	V
Horizontal input gate voltage	V_{IGH}		-10 to +15	V
Summing gate voltage	V_{SG}		-10 to +15	V
Output gate voltage	V_{OG}		-10 to +15	V
Reset gate voltage	V_{RG}		-10 to +15	V
Transfer gate voltage	V_{TG}		-10 to +15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H}		-10 to +15	V

*2: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: During high-speed operation, the temperature of the sensor increases. Take heat dissipation measures as required to prevent exceeding the absolute maximum ratings.
Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to the product within the absolute maximum ratings.

Operating conditions (Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	14	15	16	V
Reset drain voltage			V_{RD}	13	14	15	V
Anti-blooming drain voltage			V_{ABD}	13	14	15	V
Test point	Horizontal input source voltage		V_{ISH}	-	V_{RD}	-	V
	Horizontal input gate voltage		V_{IGH}	-5	-4	-	
Anti-blooming gate voltage		High	V_{ABGH}	2	5	8	V
		Low	V_{ABGL}	-4	-2	0	
Summing gate voltage		High	V_{SGH}	2	5	8	V
		Low	V_{SGL}	-5	-4	-3	
Output gate voltage			V_{OG}	3	5	7	V
Substrate voltage			V_{SS}	-	0	-	V
Reset gate voltage		High	V_{RGH}	8	9	10	V
		Low	V_{RGL}	-1	0	1	
Transfer gate voltage		High	V_{TGH}	7	8	9	V
		Low	V_{TGL}	-5	-4	-3	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	2	5	8	V
		Low	V_{P1HL}, V_{P2HL}	-5	-4	-3	
External load resistance			R_L	2.0	2.2	2.4	kΩ

Electrical characterisitics (Ta=25 °C, operating conditions: Typ., unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output signal frequency*3		fop	-	20	40	MHz
Line rate	Without electronic shutter	LRnes	-	9.5	19.2	kHz
	With electronic shutter	LRes	-	9.5	18.7	
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	220	-	pF
Anti-blooming gate capacitance		C_{ABG}	-	80	-	pF
Summing gate capacitance		C_{SG}	-	10	-	pF
Reset gate capacitance		C_{RG}	-	10	-	pF
Transfer gate capacitance		C_{TG}	-	120	-	pF
Charge transfer efficiency*4		CTE	0.99995	0.99999	-	-
DC output level*3		Vo	8	9	10	V
Output impedance*3		Zo	-	160	-	Ω
Power consumption*3 *5		P	-	100	140	mW

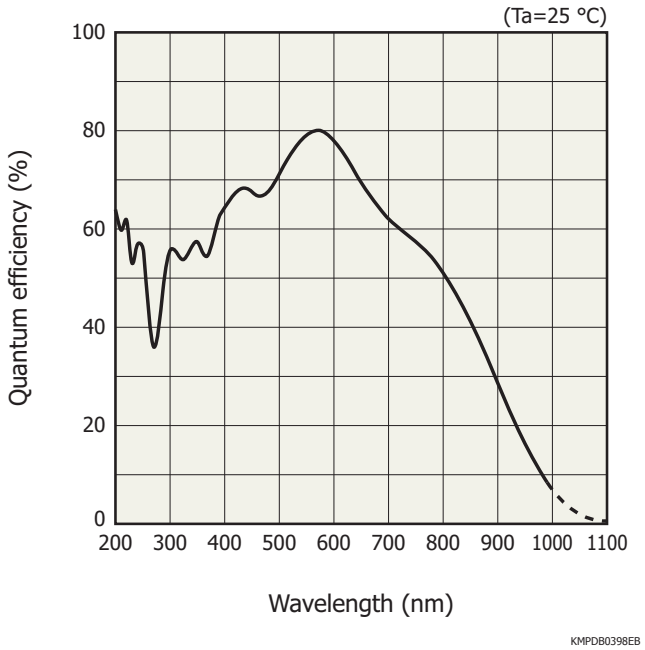
*3: The value depends on the load resistance.
*4: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity
*5: Power consumption of the on-chip amplifier plus load resistance

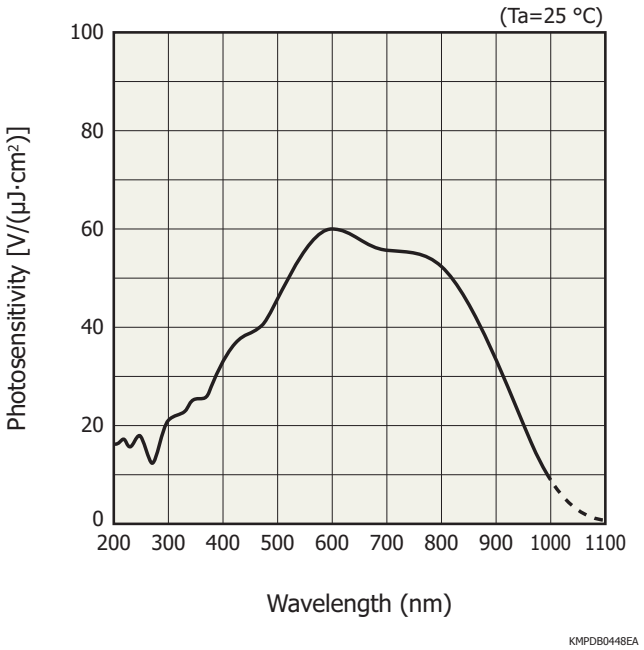
Electrical and optical characterisitics (Ta=25 °C, operating conditions: Typ., unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Csat	70	100	-	ke^-
CCD node sensitivity	CCE	11	13	15	$\mu V/e^-$
Dark current (maximum of all effective pixels)	I_D max	-	15	75	e^-/pixel/ms
Readout noise*7	Nread	-	40	60	e^- rms
Dynamic range*8	DR	1167	2500	-	-
Spectral response range	λ	-	200 to 1000	-	nm
Photoresponse nonuniformity*9 *10	PRNU	-	±3	±10	%
Image lag*9	Lag	-	0.1	1	%

*6: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*7: Readout frequency 40 MHz
*8: Dynamic range = Full well capacity / Readout noise
*9: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 470 nm)
*10: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]

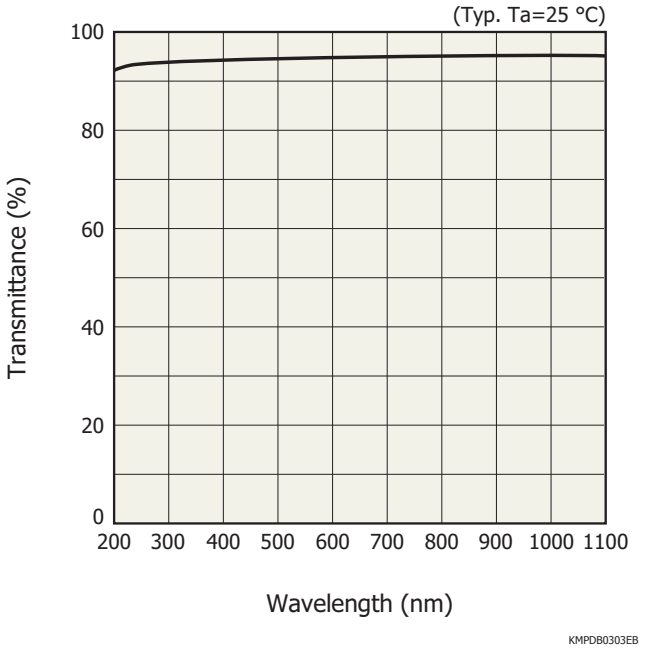
Spectral response (without window, typical example)*11



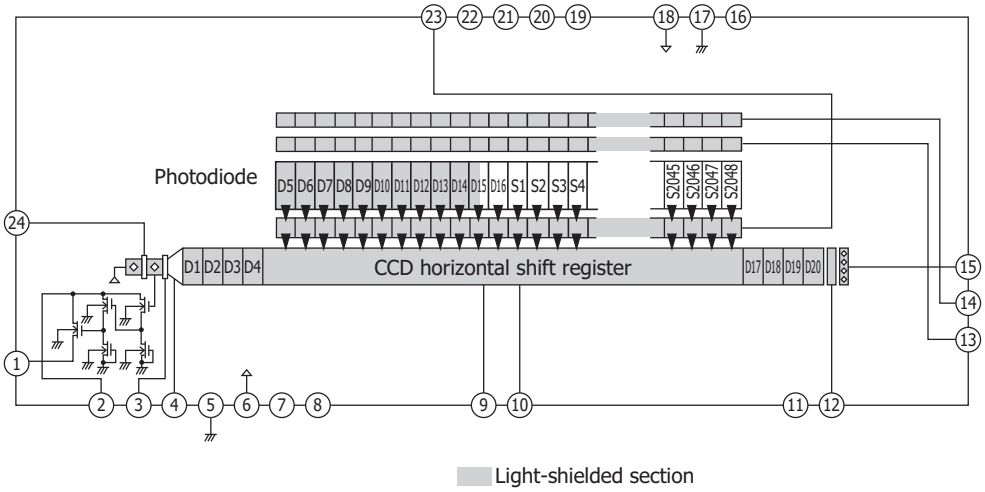


*11: Spectral response with quartz glass is decreased according to the spectral transmittance characteristics of window material.

Spectral transmittance characteristics of window material



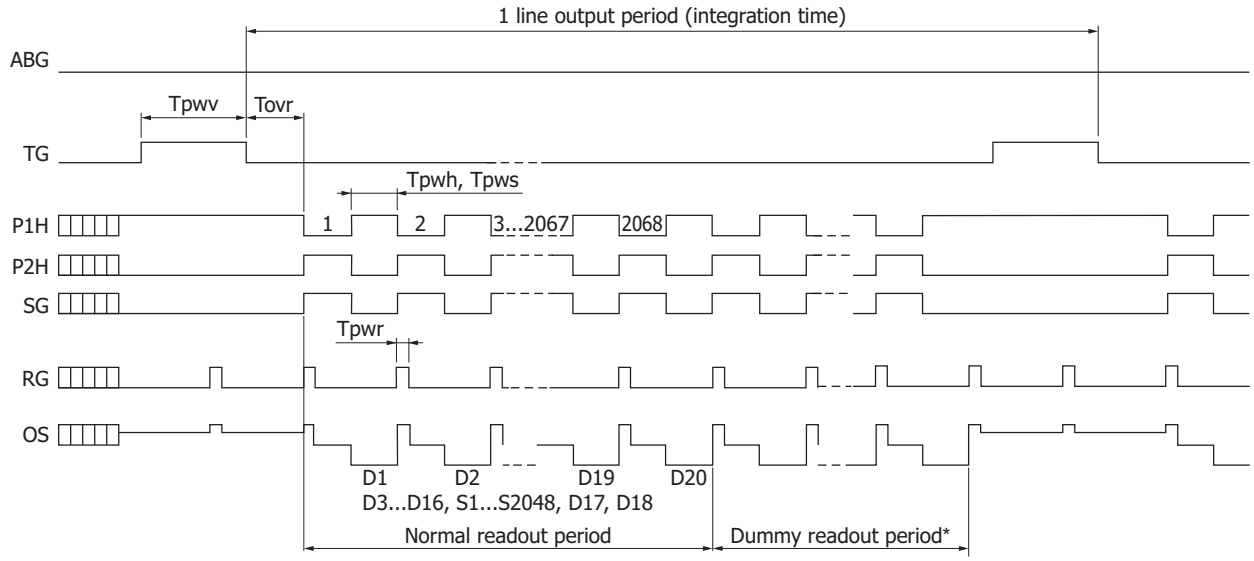
Device structure (conceptual drawing of top view in dimensional outline)



KMPDC0483EA

Timing chart

When not using electronic shutter



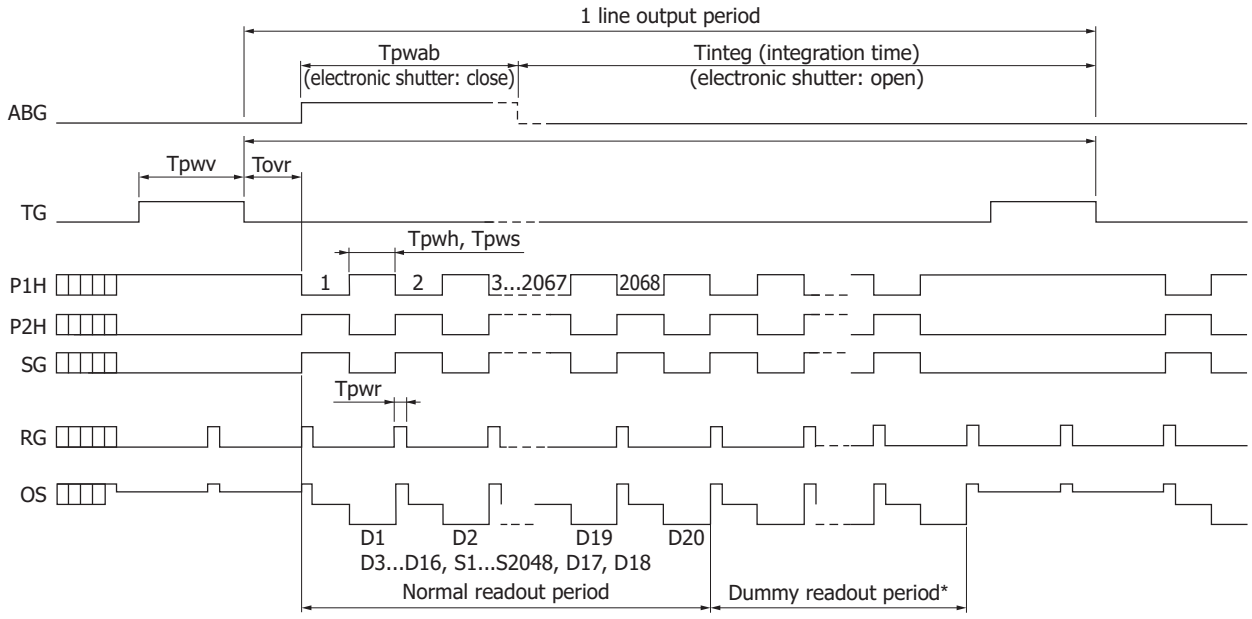
* When making the integration time longer than the normal readout period, to carry away the dark current generated in the CCD horizontal shift register, perform dummy readout after completion of the normal readout until right before rising transfer gate pulse.

KMPDC0484EB

Parameter		Symbol	Min.	Typ.	Max.	Unit
TG	Pulse width	Tpwv	0.2	0.4	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H*12	Pulse width	Tpwh	12.5	25	-	ns
	Rise and fall times	Tprh, Tpfh	2	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	12.5	25	-	ns
	Rise and fall times	Tprs, Tpfs	2	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	6	12	-	ns
	Rise and fall times	Tprr, Tpfr	1	-	-	ns
TG - P1H	Overlap time	Tovr	0.1	0.2	-	µs

*12: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

When using electronic shutter



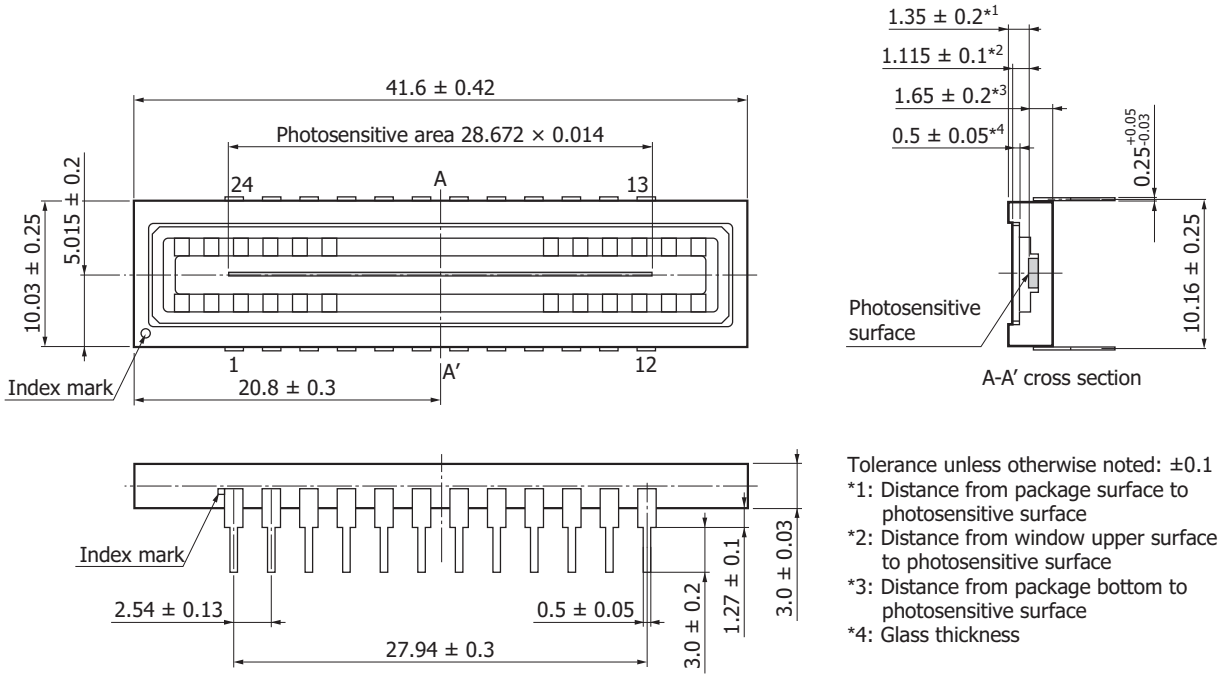
* When making the integration time longer than the normal readout period, to carry away the dark current generated in the CCD horizontal shift register, perform dummy readout after completion of the normal readout until right before rising transfer gate pulse.

KMPDC0485EB

Parameter		Symbol	Min.	Typ.	Max.	Unit
ABG	Pulse width	Tpwab	1	-	-	µs
	Rise and fall times	Tprab, Tpfab	300	-	-	ns
TG	Pulse width	Tpwv	1.6	2.0	-	µs
	Rise and fall times	Tprv, Tpfv	10	-	-	ns
P1H, P2H*13	Pulse width	Tpwh	12.5	25	-	ns
	Rise and fall times	Tprh, Tpfh	2	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	12.5	25	-	ns
	Rise and fall times	Tprs, Tpfs	2	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	6	12	-	ns
	Rise and fall times	Tprr, Tpfr	1	-	-	ns
TG - P1H	Overlap time	Tovr	0.1	0.2	-	µs
Integration time		Tinteg	2	-	-	µs

*13: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.1
*1: Distance from package surface to photosensitive surface
*2: Distance from window upper surface to photosensitive surface
*3: Distance from package bottom to photosensitive surface
*4: Glass thickness

This product is not hermetically sealed and moisture may penetrate inside the package. Avoid using or storing this product in an environment where sudden temperature and humidity changes may occur and cause condensation in the package.

KMPDA0310EA

Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P2H
5	SS	Substrate	GND
6	RD	Reset drain	+14 V
7	-		
8	-		
9	P2H	CCD horizontal resister clock-2	+5/-4 V
10	P1H	CCD horizontal resister clock-1	+5/-4 V
11	-		
12	IGH	Test point (horizontal input gate)	-4 V
13	ABG	Anti-blooming gate	+5/-2 V
14	ABD	Anti-blooming drain	+14 V
15	ISH	Test point (horizontal input source)	Connect it to RD.
16	-		
17	SS	Substrate	GND
18	RD	Reset drain	+14 V
19	-		
20	-		
21	-		
22	-		
23	TG	Transfer gate	+8/-4 V
24	RG	Reset gate	+9/0 V

Precautions

■ Electrostatic countermeasures

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ When UV light irradiation is applied

When UV light irradiation is applied, the product characteristics may degrade. Such examples include degradation of the product's UV sensitivity and increase in dark current. This phenomenon varies depending on the irradiation level, irradiation intensity, usage time, and ambient environment and also varies depending on the product model. Before employing the product, we recommend that you check the tolerance under the ultraviolet light environment that the product will be used in.

Related information

www.hamamatsu.com/sp/ssd/doc_ja.html

■ Precautions
· Disclaimer
· Image sensors

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Cat. No. KMPD1147E04 Oct. 2016 DN