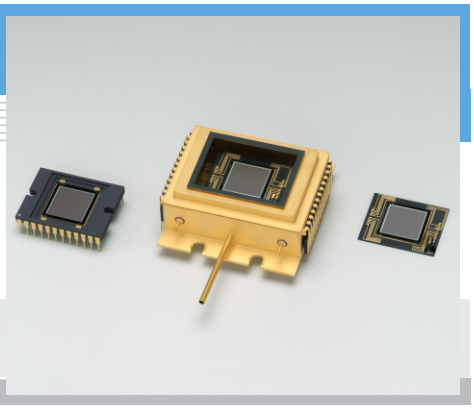

CCD area image sensor
S9737 series

1024 × 1024 pixels, front-illuminated FFT-CCDs

S9737 series is a family of FFT-CCD area image sensors specifically designed for low-light-level detection in scientific applications. S9737 series also features low noise and low dark current (MPP mode operation). These enable low-light-level detection and long integration time, thus achieving a wide dynamic range.
Three different packages (ceramic DIP, metal, plate type) are provided. Metal package type (S9737-02) has a four-stage TE-cooled element built into the same package for thermoelectric cooling. At room temperature operation, the device can be cooled down to -70 ˚C with using forced air cooling. In addition, since both the CCD chip and TE-cooled element are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- 1024 (H) × 1024 (V) pixel format
- Pixel size: 12 × 12 µm
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation
- 3 types of packages are available

Applications

- Astronomy
- Scientific measuring instrument
- Fluorescence spectrometer
- Raman spectrophotometer
- Optical and spectrophotometric analyzer
- For low-light-level detection requiring

■ General ratings

Parameter	S9737-01	S9737-02	S9737-03
CCD structure	Full frame transfer		
Fill factor	100 %		
Number of active pixels	1024 (H) × 1024 (V)		
Pixel size	12 (H) × 12 (V) µm		
Active area	12.288 (H) × 12.288 (V) mm		
Vertical clock phase	2 phase		
Horizontal clock phase	2 phase		
Output circuit	One-stage MOSFET source follower		
Cooling	Non-cooled	Four-stage TE-cooled	Non-cooled
Package	24-pin ceramic DIP	28-pin metal package	Plate type
Window	None (covered with tape)	AR coated Sapphire	None

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
CCD cooling temperature	-	-70	-	+30	°C
Output transistor drain voltage	V_{OD}	-0.5	-	+25	V
Reset drain voltage	V_{RD}	-0.5	-	+18	V
Test point (vertical input source)	V_{ISV}	-0.5	-	+18	V
Test point (horizontal input source)	V_{ISH}	-0.5	-	+18	V
Test point (vertical input gate)	V_{IG1V}, V_{IG2V}	-15	-	+15	V
Test point (horizontal input gate)	V_{IG1H}, V_{IG2H}	-15	-	+15	V
Summing gate voltage	V_{SG}	-15	-	+15	V
Output gate voltage	V_{OG}	-15	-	+15	V
Reset gate voltage	V_{RG}	-15	-	+15	V
Transfer gate voltage	V_{TG}	-15	-	+15	V
Vertical shift register clock voltage	V_{P1V}, V_{P2V}	-15	-	+15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H}	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	12	13	14	V
Output gate voltage		V_{OG}	-0.5	2	-	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	0	3	6	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	0	3	6	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	0	3	6	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	0	3	6	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	0	3	6	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	0.1	1	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	-	6000	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	-	200	-	pF
Summing gate capacitance	C_{SG}	-	-	5	-	pF
Reset gate capacitance	C_{RG}	-	-	5	-	pF
Transfer gate capacitance	C_{TG}	-	-	50	-	pF
Transfer efficiency	CTE	*1	0.99995	0.99999	-	-
DC output level	Vout	*2	12	15	18	V
Output impedance	Zo	*2	-	3	-	kΩ
Power dissipation	P	*2, *3	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*2: The values depend on the load resistance. (V_{OD}=20 V, Load resistance=22 kΩ)
*3: Power dissipation of the on-chip amplifier.

■Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	-	30	60	-	ke⁻
	Horizontal			-	72	-	
CCD node sensitivity		Sv	*4	-	4.5	-	μV/e⁻
Dark current (MPP mode)	+25 °C	DS	*5	-	100	1500	e⁻/pixel/s
	0 °C			-	5	75	
	-70 °C			-	0.0005	0.005	
Readout noise		Nr	*6	-	4	18	e⁻rms
Dynamic range (Area scanning)			*7	-	15000	-	-
Spectral response range		λ	-	-	400 to 1100	-	nm
Photo response non-uniformity		PRNU	*8	-	-	±10	%
Blemish	Point defects	-	*9	-	-	0	-
	Cluster defects		*10	-	-	0	
	Column defects		*11	-	-	0	

*4: VOD=20 V , Load resistance=22 kΩ
*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*6: -40 °C, operating frequency is 80 kHz.
*7: DR = Fw / Nr
*8: Measured at half of the full well capacity. PRNU = noise / signal × 100 [%], noise: fixed pattern noise (peak to peak)
*9: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels
*10: A group of 2 to 9 continuous point defects
*11: A group of 10 or more continuous point defects

■ Pin connections (S9737-01)

Pin No.	Symbol	Description	Remark
1	RG	Reset gate	-
2	RD	Reset drain	-
3	OS	Output source	-
4	OD	Output transistor drain	-
5	OG	Output gate	-
6	SG	Summing gate	-
7	P2H	CCD horizontal register clock-2	-
8	NC	No connection	-
9	P1H	CCD horizontal register clock-1	-
10	NC	No connection	-
11	IG2H	Test point (horizontal input gate-2)	Shorted to ground
12	IG1H	Test point (horizontal input gate-1)	Shorted to ground
13	ISH	Test point (horizontal input source)	Shorted to RD
14	TG	Transfer gate	-
15	P2V	CCD vertical register clock-2	-
16	NC	No connection	-
17	P1V	CCD vertical register clock-1	-
18	NC	No connection	-
19	NC	No connection	-
20	SS	Substrate (GND)	-
21	NC	No connection	-
22	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	Shorted to ground
24	IG1V	Test point (vertical input gate-1)	Shorted to ground

■ Pin connections (S9737-02)

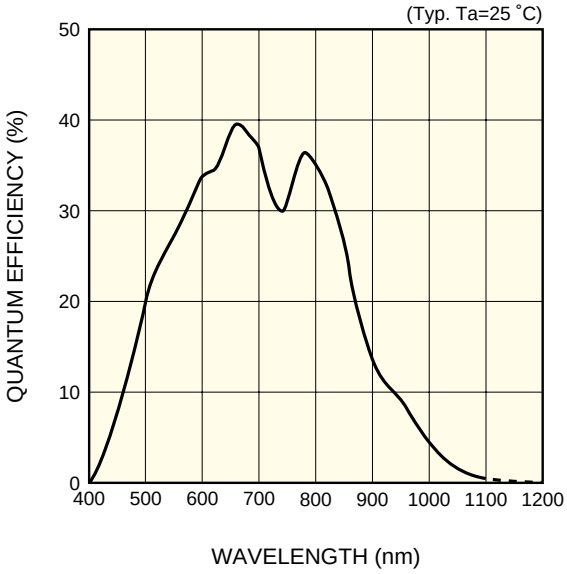
Pin No.	Symbol	Description	Remark
1	P-	TE-cooler-	
2	NC		
3	SS	Substrate (GND)	
4	NC		
5	ISV	Test point (vertical input source)	Shorted to RD
6	IG2V	Test point (vertical input gate-2)	Shorted to 0 V
7	IG1V	Test point (vertical input gate-1)	Shorted to 0 V
8	RG	Reset gate	
9	RD	Reset drain	
10	OS	Output transistor source	
11	OD	Output transistor drain	
12	OG	Output gate	
13	SG	Summing gate	Same timing as P2H
14	P+	TE-cooler+	
15	TSH1	Temperature sensor (hot side)	
16	TSC1	Temperature sensor (cool side)	
17	TSC2	Temperature sensor (cool side)	
18	P2H	CCD horizontal register clock-2	
19	P1H	CCD horizontal register clock-1	
20	IG2H	Test point (horizontal input gate-2)	Shorted to 0 V
21	IG1H	Test point (horizontal input gate-1)	Shorted to 0 V
22	ISH	Test point (horizontal input source)	Shorted to RD
23	P2V	CCD vertical register clock-2	
24	P1V	CCD vertical register clock-1	
25	TG	Transfer gate	Same timing as P2V *12
26	NC		
27	NC		
28	TSH2	Temperature sensor (hot side)	

■ Pad connections (S9737-03)

Pad No.	Symbol	Description	Remark
1	RG	Reset gate	
2	RD	Reset drain	
3	OS	Output transistor source	
4	OD	Output transistor grain	
5	OG	Output gate	
6	SG	Summing gate	
7	NC		
8	NC		
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	
12	IG1H	Test point (horizontal input gate-1)	
13	ISH	Test point (horizontal input source)	
14	P2V	CCD vertical resister clock-2	
15	P1V	CCD vertical resister clock-1	
16	TG	Transfer gate	Same timing as P2V*12
17	NC		
18	NC		
19	NC		
20	SS	Substrate (GND)	
21	NC		
22	ISV	Test point (vertical input source)	
23	IG2V	Test point (vertical input gate-2)	
24	IG1V	Test point (vertical input gate-1)	

*12: TG is an isolation gate between vertical register and horizontal register.
In standard operation, the same pulse of P2V should be applied to the TG.

■ Spectral response (without window)



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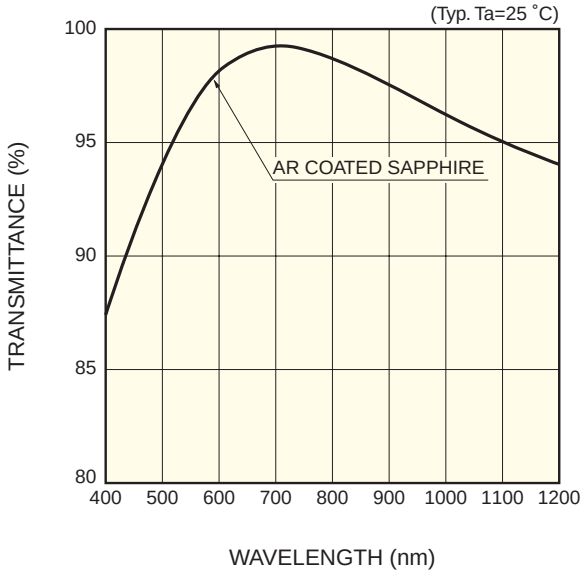
■ Spectral transmittance characteristics of window material



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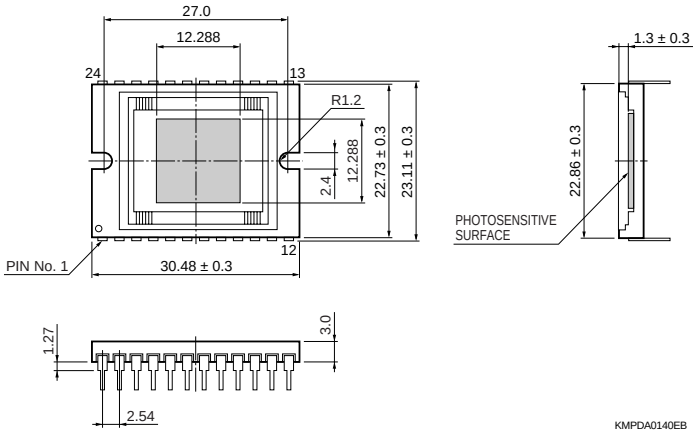
■ Dimensional outlines (unit: mm)

S9737-01



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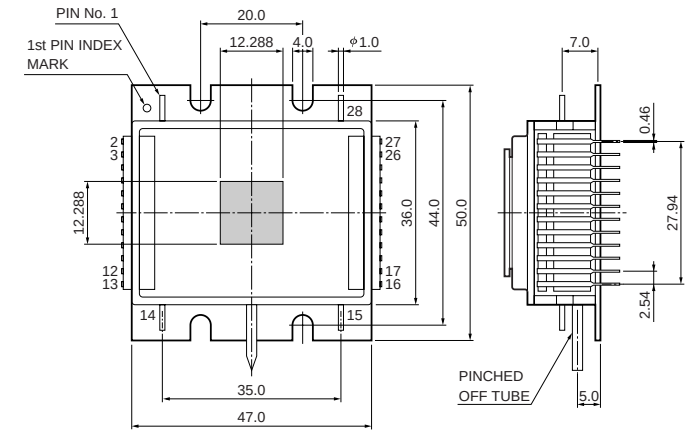
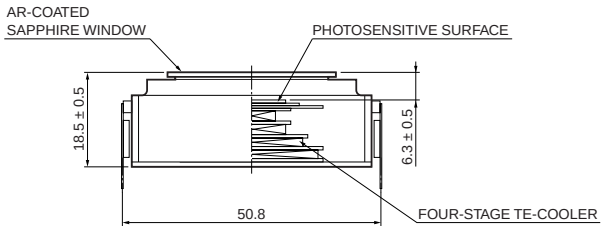
S9737-02





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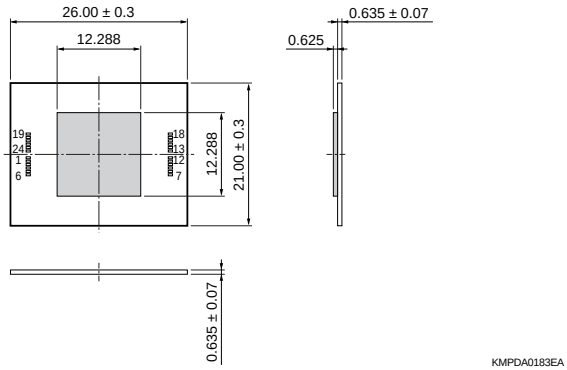
S9737-03



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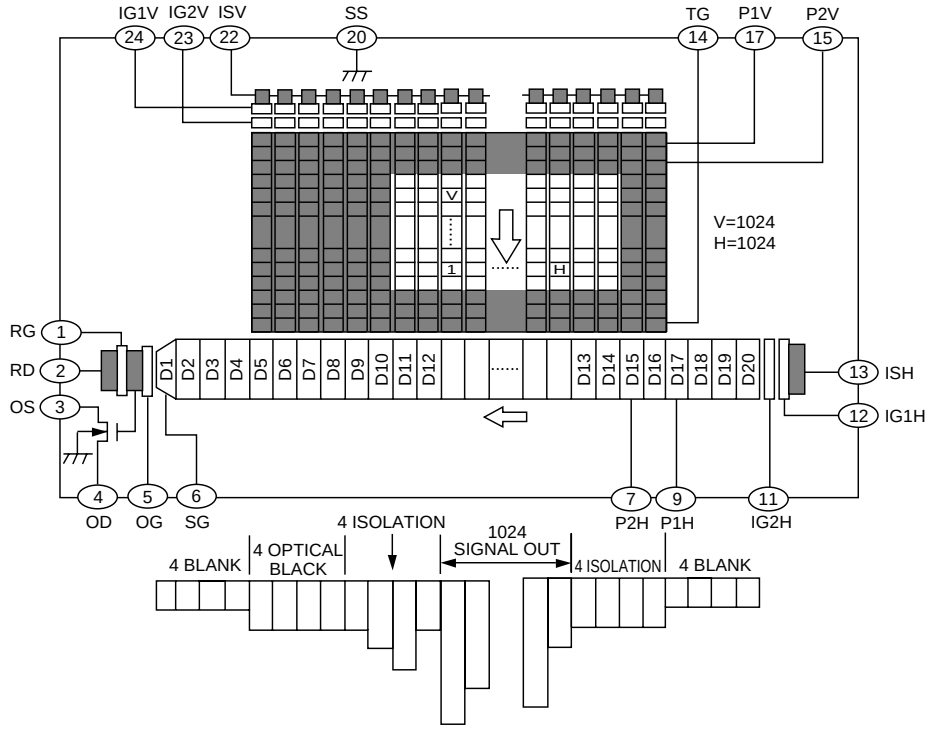
■ Device structure, line output format (S9737-01)



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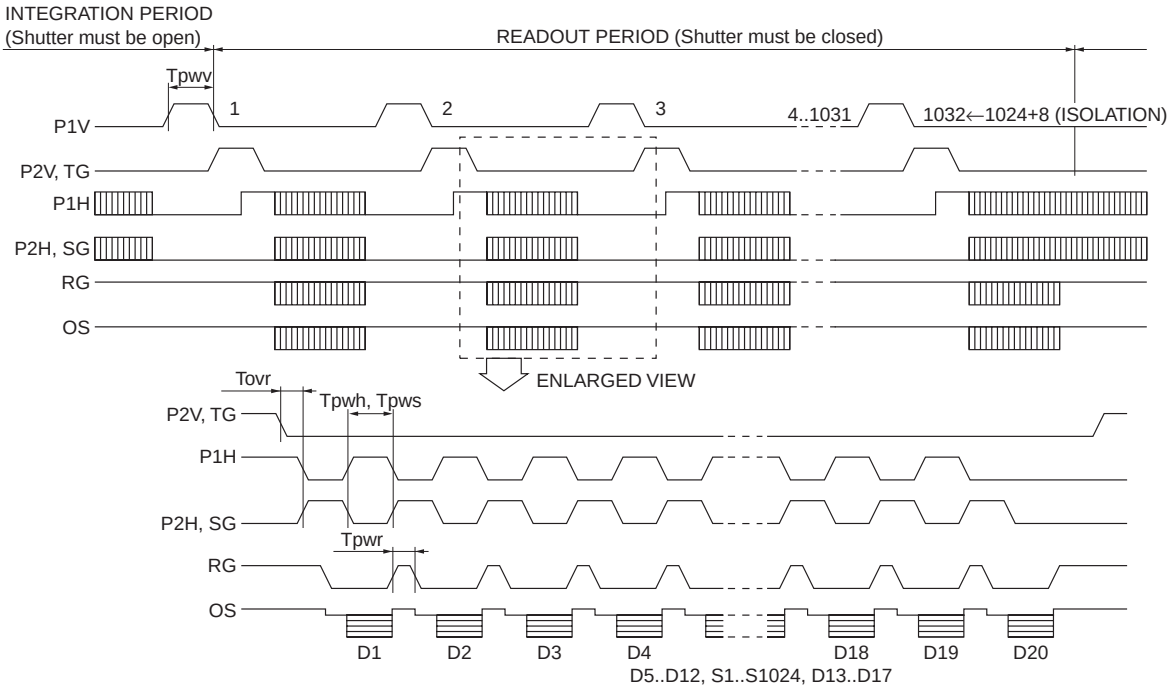
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	4	1024	4	-	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
4	1024	4

■ Timing chart

● Area scanning 1 (low dark current mode)



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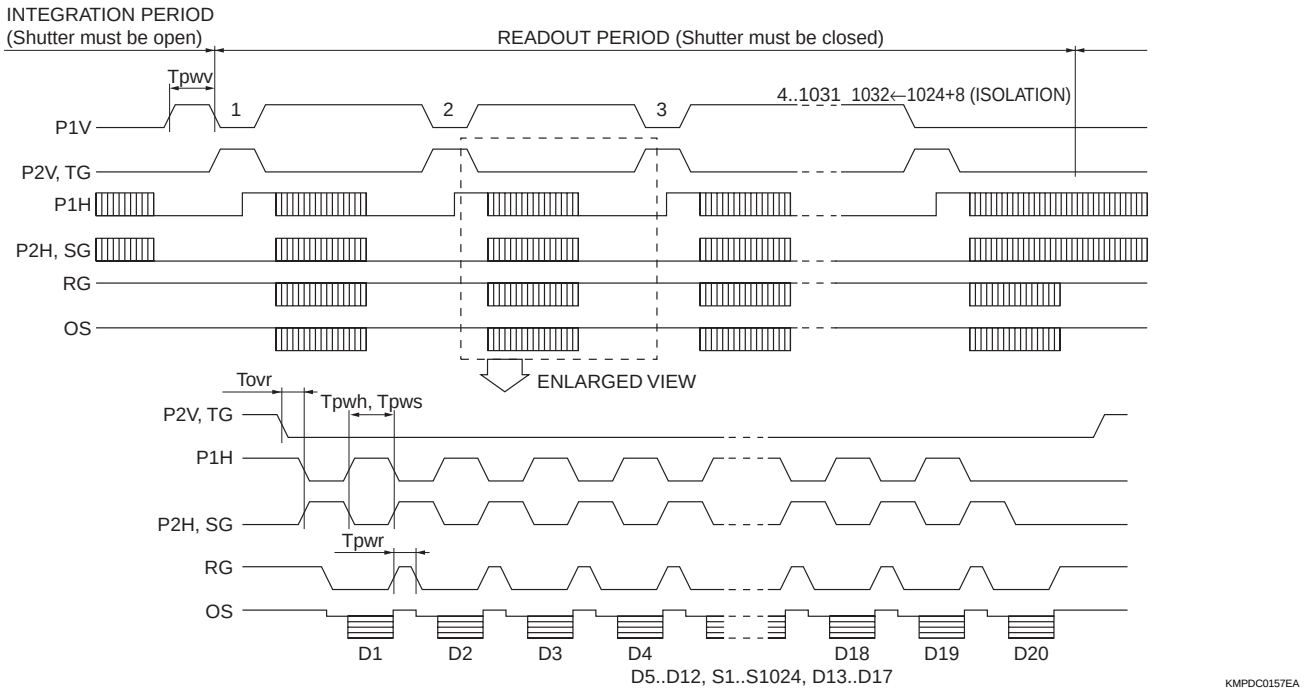
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V	Pulse width	Tpwv	*13	6	18	-	µs
P2V, TG	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*13	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	6	-	µs

*13: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

● Area scanning 2 (large full well mode)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V	Pulse width	Tpwv	*14	6	18	-	µs
P2V, TG	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*14	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	6	-	µs

*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■ Specifications of built-in TE-cooler (S9737-02)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	1.6	-	Ω
Maximum current *15	Imax	Th *16=27 °C ΔT *17=ΔTmax	-	-	4.4	A
Maximum voltage	Vmax	Th*16=27 °C ΔT=ΔTmax I=Imax	-	-	7.4	V
Maximum heat absorption *18	Qmax	Tc *19=Th *16=27 °C I=Imax	-	-	3.0	W
Maximum temperature at hot side	-		-	-	50	°C
CCD temperature	-	Ta=25 °C	-	-70	-50	°C

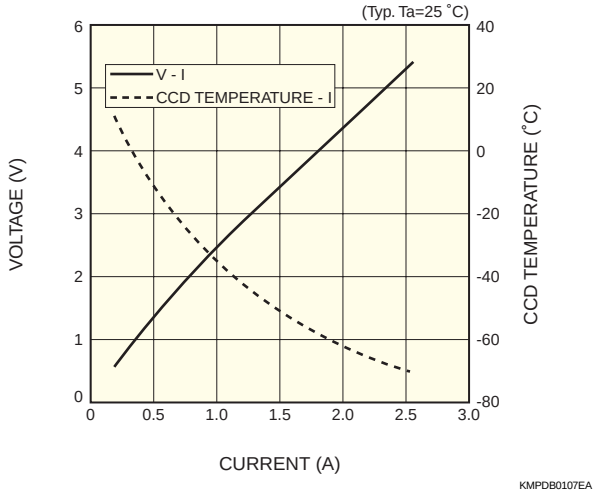
*15: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*16: Temperature at hot side of thermoelectric cooler.

*17: ΔT=Th - Tc

*18: This is a theoretical heat absorption level that offsets the temperature difference in the TE-cooled element when the maximum current is supplied to the unit.

*19: Temperature at cool side of thermoelectric cooler.



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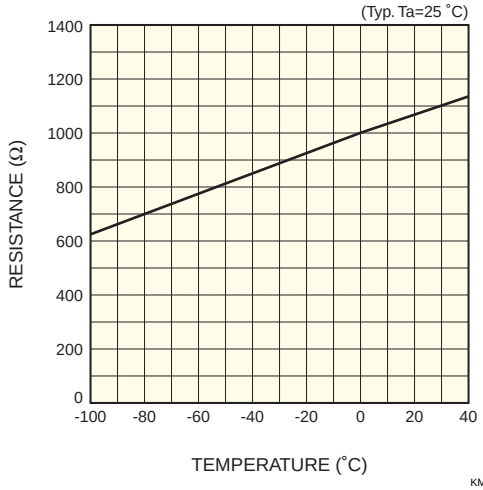
■ Specifications of built-in temperature sensors (S9737-02)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at cool side	Rc	T=0 °C	-	1000	-	Ω
Temperature coefficient of resistance at cool side	-	-	-	0.00375	-	Ω/Ω
Resistance at hot side	Rh	T=0 °C	-	1000	-	Ω
Temperature coefficient of resistance at hot side	-	-	-	0.00385	-	Ω/Ω



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■ Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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