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TDI-CCD area image sensor

S8658-01/01F

Image sensor with a long, narrow photosensitive area for X-ray imaging

The S8658-01 is an front-illuminated FFT-CCD image sensor developed for X-ray imaging. A FOS (Fiber Optic plate with Scintillator) sensitive to X-rays is directly coupled to the CCD chips, allowing X-ray imaging with high precision. Three CCD chips are arranged in close proximity to configure a long photosensitive area (approx. 220 mm).
The S8658-01 CCD image sensor features TDI operation that allows capturing clear, sharp X-ray images of objects moving on a belt conveyor, making it ideal for non-destructive X-ray inspection. FOP type not coated with scintillator material is also provided (S8658-01F).

Features

- **1536 × 128 pixel (× 3 chips)**
- **Pixel size: 48 × 48 µm**
- **Slit-like image of 220 mm long by aligning 3 CCD chips together**
- **TDI (time delay integration) operation**
- **100% fill factor**
- **Wide dynamic range**
- **Low dark current**
- **MPP operation**

Applications

- **General X-ray imaging**
- **Non-destructive inspection**
- **Dental panorama, cephalo**

Specifications

Parameter	S8658-01	S8658-01F
CCD structure	Full frame transfer or TDI	
Window	FOS (fiber optic plate with scintillator)	FOP (fiber optic plate)*1
Photosensitive area (H × V)	73.728 × 6.144 mm (× 3 chips)	
X-ray photosensitive area	220 × 6 mm	-
Pixel size (H × V)	48 × 48 µm	
Number of total pixels (H × V)	1536 × 128 pixel (× 3 chips)	
Number of effective pixels (H × V)	1536 × 128 (× 3 chips)	
Fill factor	100%	
Vertical clock phase	2 phases and 2 lines	
Horizontal clock phase	2 phases and 2 lines	
Output circuit	Two-stage MOSFET source follower with load resistance	
X-ray resolution	4 to 6 Lp/mm at 60 kVp, 20 µGy	-
Total dose irradiation	50 Gy max.	-
Package	60-pin ceramic	
Cooling	Non-cooled	

*1: When using this product for X-ray detection, the user must affix a phosphor sheet to the photosensitive area.

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	-20	-	+70	°C
Operating temperature	Topr	0	-	+40	°C
OD voltage	V_{OD}	-0.5	-	+20	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
IGV voltage	V_{IGV}	-15	-	+15	V
IGH voltage	V_{IGH}	-15	-	+15	V
SG voltage	V_{SG}	-15	-	+15	V
OG voltage	V_{OG}	-15	-	+15	V
RG voltage	V_{RG}	-15	-	+15	V
TG voltage	V_{TG}	-15	-	+15	V
Vertical clock voltage	V_{P1AV}, V_{P2AV} V_{P1BV}, V_{P2BV}	-15	-	+15	V
Horizontal clock voltage	V_{P1AH}, V_{P2AH} V_{P1BH}, V_{P2BH}	-15	-	+15	V

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	15	18	V
Reset drain voltage			V_{RD}	12	13	14	V
Output gate voltage			V_{OG}	-0.5	2	5	V
Output transistor ground voltage			V_{SSA}	-	0	-	V
Substrate voltage			V_{SSD}	-5	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Vertical input gate		V_{IGV}	-8	0	-	
	Horizontal input gate		V_{IGH}	-8	0	-	
Vertical shift register clock voltage		High	V_{P1AVH}, V_{P2AVH} V_{P1BVH}, V_{P2BVH}	0	3	6	V
		Low	V_{P1AVL}, V_{P2AVL} V_{P1BVL}, V_{P2BVL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1AHH}, V_{P2AHH} V_{P1BHH}, V_{P2BHH}	0	3	6	V
		Low	V_{P1AHL}, V_{P2AHL} V_{P1BHL}, V_{P2BHL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	0	3	6	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	0	3	6	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	0	3	6	V
		Low	V_{TGL}	-9	-8	-7	

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	C_{P1AV}, C_{P2AV} C_{P1BV}, C_{P2BV}		-	15000	-	pF
Horizontal shift register capacitance	C_{P1AH}, C_{P2AH} C_{P1BH}, C_{P2BH}		-	500	-	pF
Summing gate capacitance	C_{SG}		-	15	-	pF
Reset gate capacitance	C_{RG}		-	10	-	pF
Transfer gate capacitance	C_{TG}		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3 *4	-	60	-	mW

*2: Measured at half of the full well capacity. CTE is defined per pixel.
*3: V_{OD}=15 V
*4: Power dissipation of the on-chip amplifier (each chip)

Electrical and optical characteristics (Ta=25 °C unless otherwise noted)

Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat		-	Fw × Sv	-	V
Full well capacity		Vertical	Fw		600	1200	-	ke⁻
		Horizontal			600	1200	-	
		Summing			600	1200	-	
CCD node sensitivity			Sv	*5	0.45	0.6	-	μV/e⁻
Dark current (MPP mode)			DS	*6	-	8	24	ke⁻/pixel/s
Readout noise		Ta=25 °C	Nr	*7	-	90	-	e⁻rms
		Ta=-40 °C			-	60	120	
Dynamic range			DR	*8	5000	20000	-	
X-ray response nonuniformity (S8658-01)			XRNU	*9	-	±10	±30	%
Photo response nonuniformity (S8658-01F)			PRNU	*10				
Blemish	Point defects*11	White spots	-		-	-	10	-
		Black spots			-	-	10	
	Cluster defects			*12	-	-	0	
	Column defects			*13	-	-	0	
X-ray resolution (S8658-01)			ΔR		4	6	-	Lp/mm

*5: VOD=15 V
*6: Dark current doubles for every 5 to 7 °C.
*7: Operating frequency=2 MHz
*8: Dynamic range = Full well capacity / Readout noise
*9: X-ray irradiation of 60kVp, measured at half of the full well capacity
Measuring region that is within 146.0 mm (H) × 6.0 mm (V) (refer to dimensional outline)

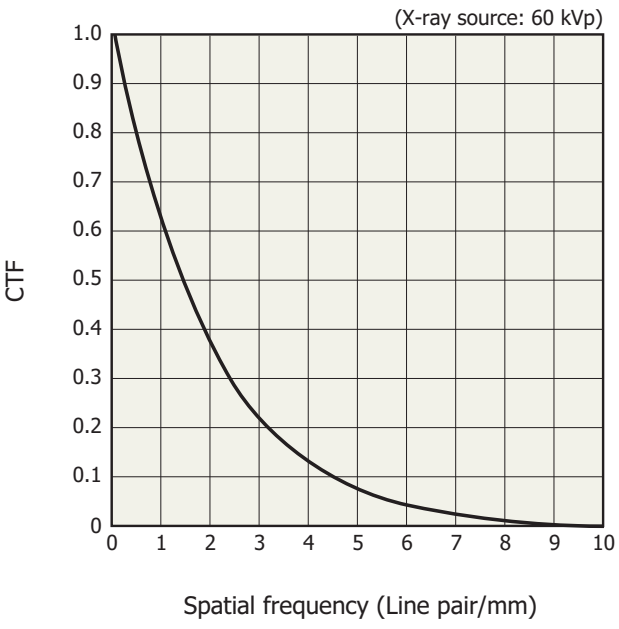
$$\text{XRNU [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 565 nm)

$$\text{PRNU [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*11: White spots > 20 times of typ. dark signal (8 ke⁻/pixel/s)
Black spots > 50% reduction in response relative to adjacent pixels, measured at half of the full well capacity
*12: continuous 2 to 9 point defects
*13: continuous >10 point defects

Resolution (S8658-01)



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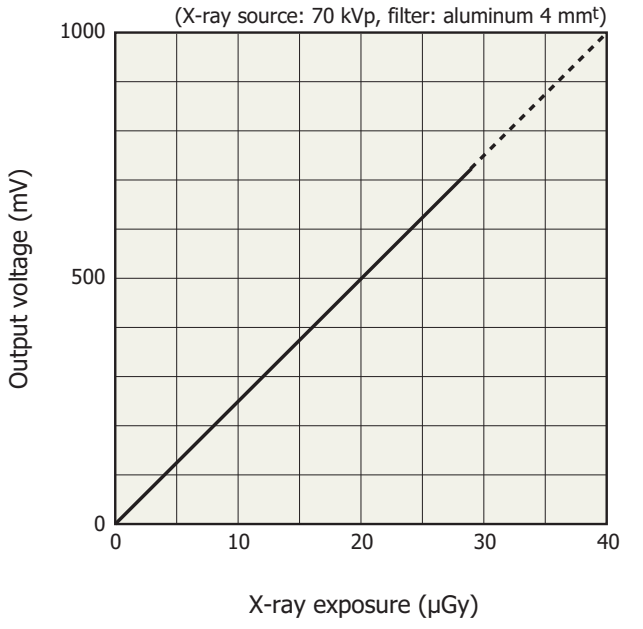
Output voltage vs. X-ray exposure (S8658-01)



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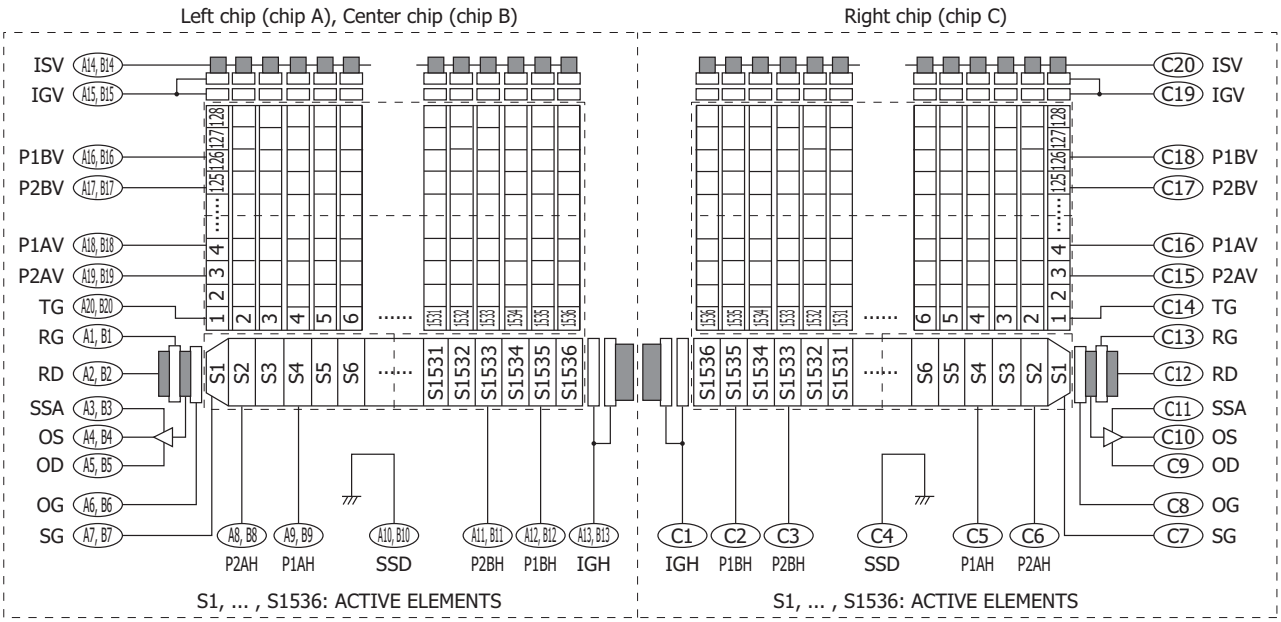
Device structure



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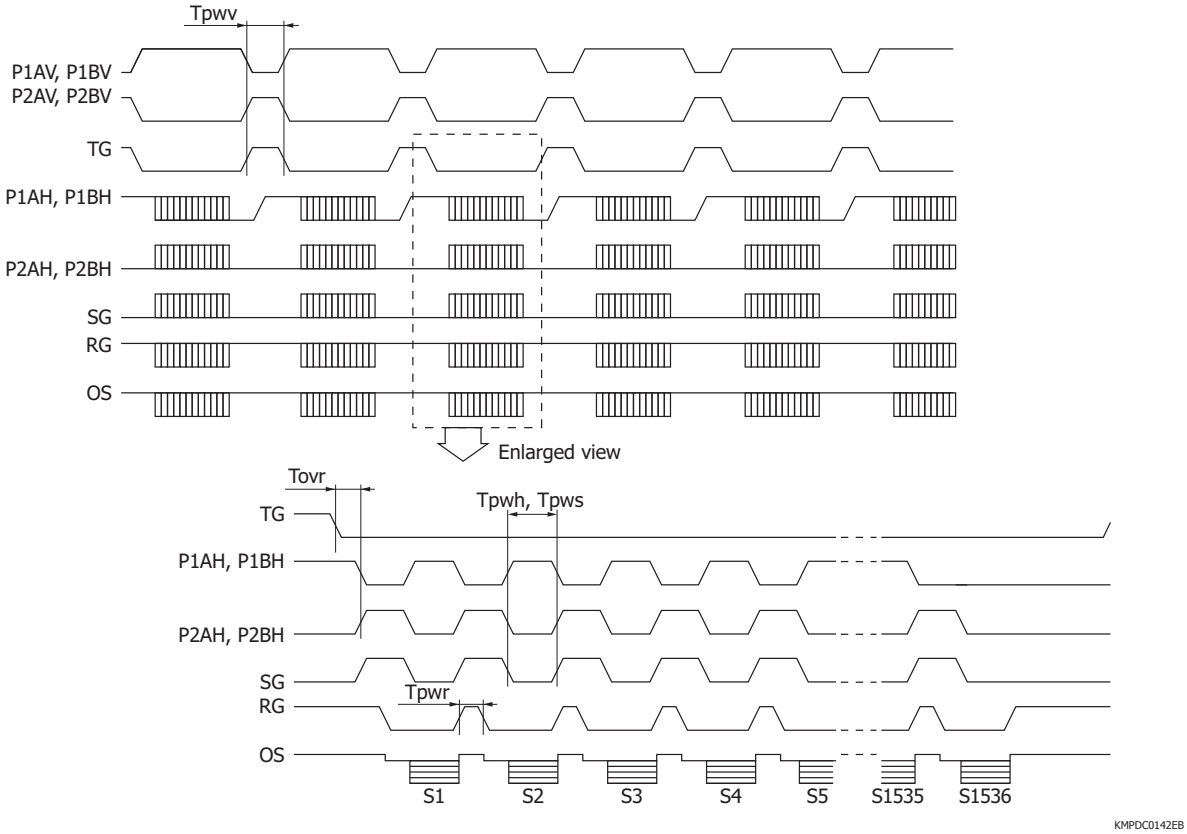
Pixel format

← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

Top ← Horizontal Direction → Right		
Isolation	Effective	Isolation
0	128	0

Timing chart (TDI operation)



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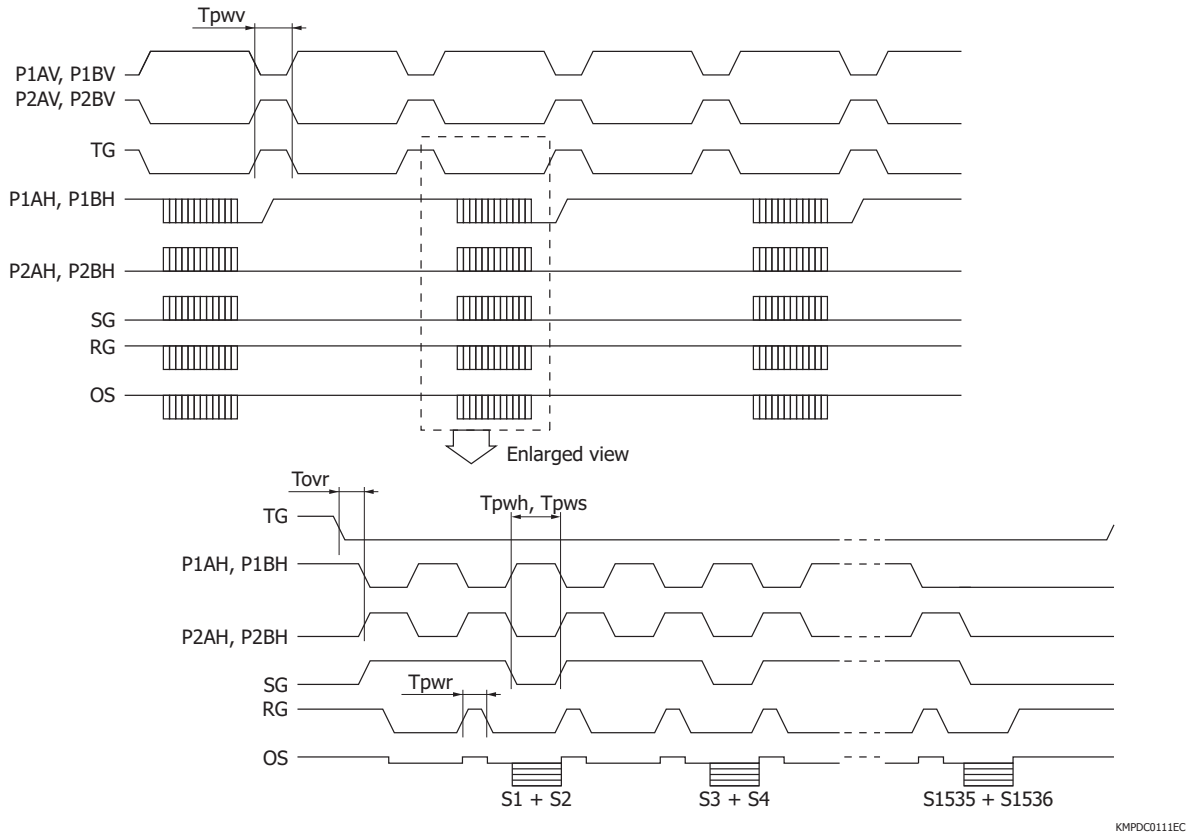
Timing chart (TDI operation, 2 × 2 pixel binning)

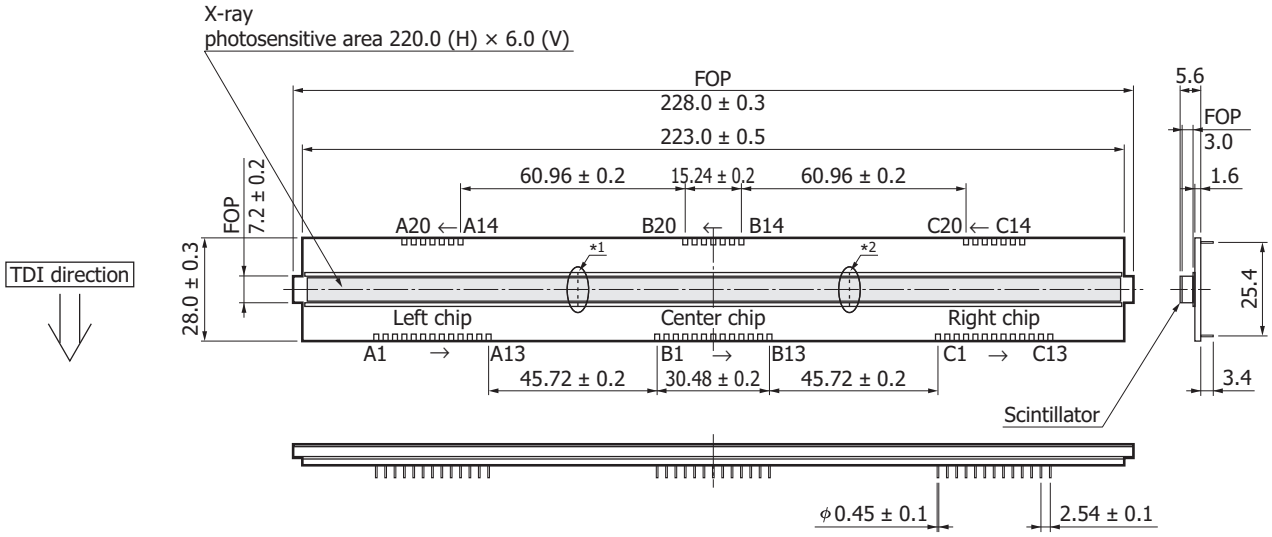


Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1AV, P1BV, P2AV, P2BV, TG	Pulse width	tpwv	*16 *17	30	60	-	µs
	Rise and fall times	tprv, tpfv		200	-	-	ns
P1AH, P1BH, P2AH, P2BH	Pulse width	tpwh	*17	125	250	-	ns
	Rise and fall times	tprh, tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	tpws		125	250	-	ns
	Rise and fall times	tprs, tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	tpwr		10	50	-	ns
	Rise and fall times	tprr, tpfr		5	-	-	ns
TG-P1AH, P1BH	Overlap time	tovr		10	20	-	µs

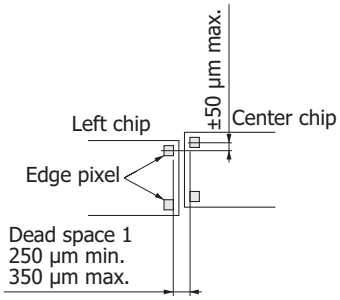
*16: TG terminal can be short-circuited to P2AV terminal.
*17: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

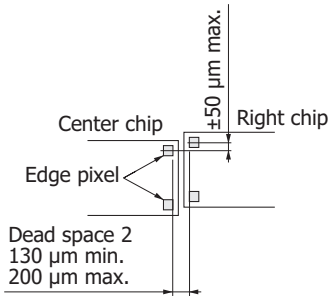
S8658-01



*1 details



*2 details



Tolerance (unless otherwise noted)

	<1 mm	: ±0.2 mm
1≤ to	<5 mm	: ±0.5 mm
5mm ≤		: ±1.0 mm

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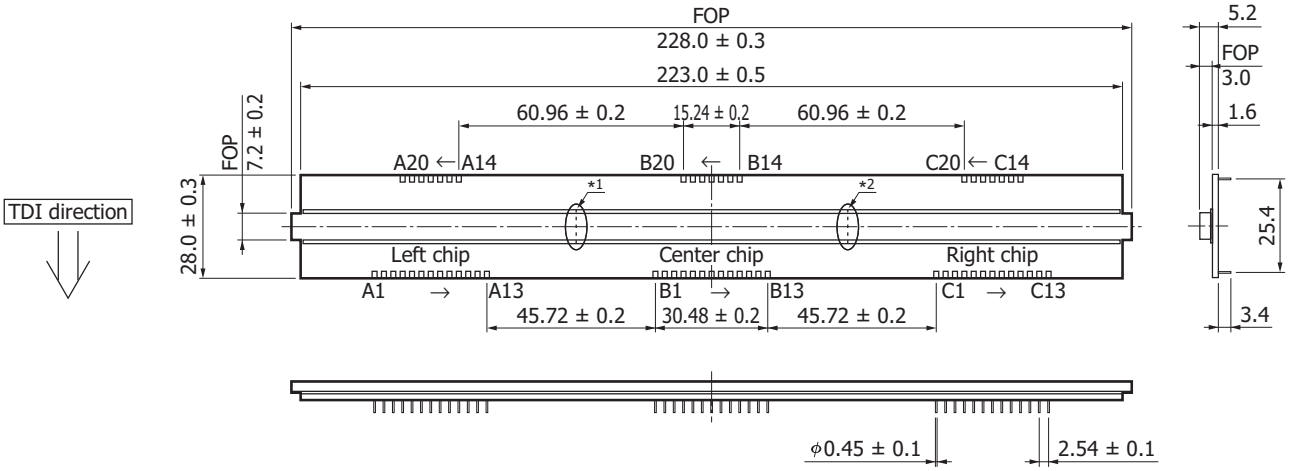
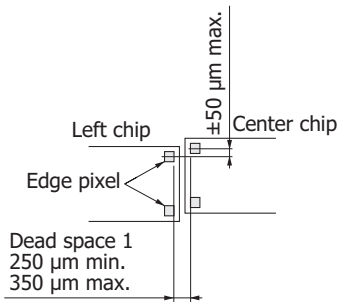
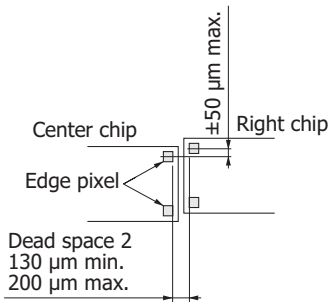
S8658-01F



*1 details



*2 details



Tolerance (unless otherwise noted)

	<1 mm	: ±0.2 mm
1≤	to <5 mm	: ±0.5 mm
5 mm ≤		: ±1.0 mm

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Pin connections

Pin no.	Symbol	Description	Remark
A1, B1	RG	Reset gate	
A2, B2	RD	Reset drain	
A3, B3	SSA	Analog ground	
A4, B4	OS	Output transistor source	
A5, B5	OD	Output transistor drain	
A6, B6	OG	Output gate	
A7, B7	SG	Summing gate	
A8, B8	P2AH	CCD horizontal register clock A-2	
A9, B9	P1AH	CCD horizontal register clock A-1	
A10, B10	SSD	Digital ground	
A11, B11	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
A12, B12	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
A13, B13	IGH	Test point (horizontal input gate)	
A14, B14	ISV	Test point (vertical input source)	Shorted to RD
A15, B15	IGV	Test point (vertical input gate)	
A16, B16	P1BV	CCD vertical register clock B-1	Same timing as P1AV
A17, B17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
A18, B18	P1AV	CCD vertical register clock A-1	
A19, B19	P2AV	CCD vertical register clock A-2	
A20, B20	TG	Transfer gate	
C1	IGH	Test point (horizontal input gate)	
C2	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
C3	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
C4	SSD	Digital ground	
C5	P1AH	CCD horizontal register clock A-1	
C6	P2AH	CCD horizontal register clock A-2	
C7	SG	Summing gate	
C8	OG	Output gate	
C9	OD	Output transistor drain	
C10	OS	Output transistor source	
C11	SSA	Analog ground	
C12	RD	Reset drain	
C13	RG	Reset gate	
C14	TG	Transfer gate	
C15	P2AV	CCD vertical register clock A-2	
C16	P1AV	CCD vertical register clock A-1	
C17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
C18	P1BV	CCD vertical register clock B-1	Same timing as P1AV
C19	IGV	Test point (vertical input gate)	
C20	ISV	Test Point (vertical input source)	Shorted to RD

Precautions (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use an anti-static wrist band, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Take these measures as needed to prevent electrostatic damage to the sensor.

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