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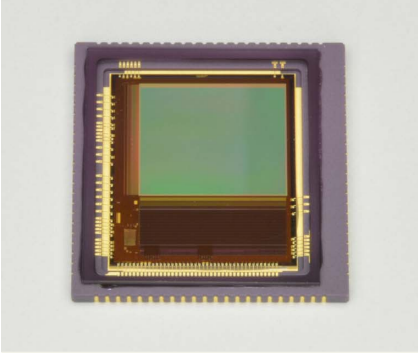
NEW

CMOS area image sensor



S13101

Near infrared high sensitivity, APS (active pixel sensor) type

The S13101 is an APS type CMOS area image sensor that has high sensitivity in the near infrared region. The pixel format is SXGA (1280 × 1024 pixels). In addition, imaging is possible at a maximum rate of 146 frames/s.
It is an all-digital I/O type with built-in timing generator, bias generator, amplifier, and A/D converter. Rolling shutter readout or global shutter readout can be selected.

Features

- **Pixel size: 7.4 × 7.4 µm**
- **Number of pixels: 1280 × 1024 (SXGA)**
- **High-speed readout: 146 frames/s max.**
- **SPI communication function (partial readout, gain switching, frame start mode selection, etc.)**
- **Rolling/global shutter readout**

Applications

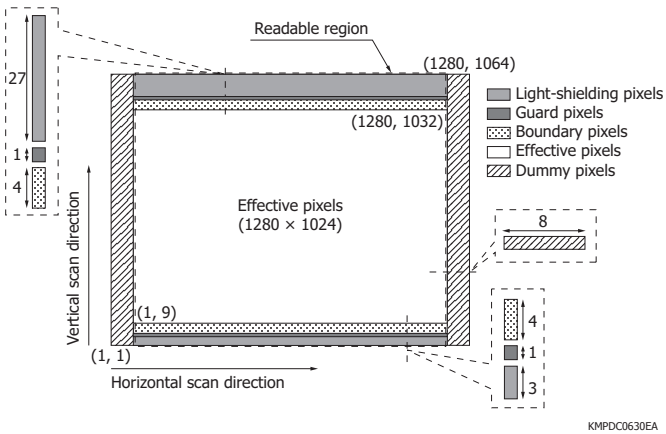
- **Machine vision**
- **Tracking**
- **Security (infrared camera)**
- **Position and shape recognition of infrared light spot**

Structure

Parameter	Specification	Unit
Image size (H × V)	9.472 × 7.578	mm
Pixel size	7.4 × 7.4	µm
Pixel pitch	7.4	µm
Total number of pixels (H × V)	1296 × 1064	pixels
Number of effective pixels (H × V)	1280 × 1024	pixels
Boundary pixels*1	4 columns enclosing the effective pixel region	-
Guard pixels*2	Rows 4 and 1037	
Light-shielding pixels*3	Rows 1 to 3 and rows 1038 to 1064	
Package	Ceramic	-
Window material	Borosilicate glass	-

*1: Same pixels as the effective pixels
*2: Pixels with a fixed photodiode potential
*3: Pixels whose photodiodes are shielded with metal

Pixel layout



Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
	Counter terminal	Vdd(C)		-0.3 to +3.9	V
Digital input signal terminal voltage*4		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage*5		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage*6		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*7	-40 to +85	°C
Storage temperature		Tstg	No dew condensation*7	-40 to +85	°C
Reflow soldering conditions*8 *9		Tsol		Peak temperature 260 °C, 3 times (see P.11)	-

*4: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST
*5: Because voltage is generated inside the chip, there is no need to supply voltage externally. To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*6: Voltage is generated inside the chip, but to improve image quality, supply an external bias voltage (-1.5 V, 2 mA). To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*7: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*8: JEDEC level 4
*9: If the microlenses formed on the photosensitive area are exposed to high temperatures such as from reflow, the sensitivity in the 600 nm and lower spectral range may degrade. The higher the temperature or the longer the exposure, the greater the degree of degradation. As such, apply reflow for a short period of time, and avoid extraneous thermal load.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.0	3.3	3.6	V
	Digital terminal	Vdd(D)	3.0	Vdd(A)	3.6	V
	Counter terminal	Vdd(C)	2.2	2.5	3.6	V
Digital input voltage*10	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.25	
Vref_cp2 terminal voltage		Vref_cp2	-2.0	-1.5	-1.0	V

*10: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST, Pll_reset

Electrical characteristics

■ Digital input signal [Ta=25 °C, recommended operating condition Typ. value (P.2), unless otherwise noted]*11

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency	f(MCLK)	25	30	35	MHz
Master clock pulse duty cycle	D(MCLK)	45	50	55	%
SPI clock pulse frequency	f(SCLK)	-	-	10	MHz
Rise time*12	tr(sigi)	-	5	7	ns
Fall time*12	tf(sigi)	-	5	7	ns

*11: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST, Pll_reset
*12: Time for the input voltage to rise or fall between 10% and 90%

■ Digital output signal [Ta=25 °C, recommended operating condition Typ. value (P.2), unless otherwise noted]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Video data rate		VR		f(MCLK) × 10		Hz
Pixel sync signal (pclk) frequency		f(pclk)		f(MCLK) × 8		Hz
Digital output voltage (LVDS output)*13	Offset	Vofs	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	V
Rise time (LVDS output)*13*14		tr(out)	-	-	2	ns
Fall time (LVDS output)*13*14		tf(out)	-	-	2	ns
Digital output voltage (CMOS output)*15	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.2	V
	Low	Vsigo(L)	-	0	0.25	V
Rise time (CMOS output)*15*16		tr(sigo)	-	10	12	ns
Fall time (CMOS output)*15*16		tf(sigo)	-	10	12	ns

*13: Pixel sync signal (pclk), line sync signal (Hsync), frame sync signal (Vsync), parallelization signal (CTR), pixel outout (Out A to Out E) When 100 Ω is connected across the LVDS output terminals.
*14: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal.
*15: SPI_MISO
*16: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal.

■ Current consumption [Ta=25 °C, recommended operating condition Typ. value (P.2), digital input signal Typ. value (P.2), unless otherwise noted]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Sum of analog and digital terminals*17	I1	-	280	380	mA
Counter terminal*17	I2	-	210	330	

*17: dark state, master clock pulse frequency=30 MHz, high-speed type, load capacitance of each output terminal=5 pF

Electrical characteristics of A/D converter [Ta=25 °C, recommended operating condition Typ. value (P.2), digital input signal Typ. value (P.2), unless otherwise noted]

■ High-precision mode (SPI value: DAC_N=3, TG_N=19)

Parameter	Symbol	Specification	Unit
Resolution	RESO	12	bit
A/D resolution	-	0.31	mV/DN

■ High-speed mode (SPI value: DAC_N=0, TG_N=3)

Parameter	Symbol	Specification	Unit
Resolution	RESO	10	bit
A/D resolution	-	1.25	mV/DN

Electrical and optical characteristics [Ta=25 °C, recommended operating condition Typ. value (P.2), digital input signal Typ. value (p.2), MCLK=30 MHz, gain: default value, offset: default value, rolling shutter, integration time=14 ms, unless otherwise noted]

■ Common to all modes

Parameter			Symbol	Min.	Typ.	Max.	Unit
Spectral response range			λ		400 to 1100		nm
Peak sensitivity wavelength			λp	-	700	-	nm
Photoresponse nonuniformity*18			PRNU	-	-	4	%
Defective pixels	Point defect	White spot*19	WS	-	-	10	pixels
		Black spot*20	BS	-	-	10	pixels
	Cluster defect*21		ClsD	-	-	0	pcs

*18: Output nonuniformity when white uniform light at 50% saturation is applied.
This is calculated excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels and is defined as follows:
PRNU = (ΔX/X) × 100 [%]
ΔX: standard deviation, X: average output of all pixels
*19: Pixels with dark output exceeding 1500 DN/s in rolling shutter mode when gain is 1 (excluding boundary pixels and guard pixels)
*20: Pixels whose output value is 50% or less than that of adjacent pixels when white uniform light at 50% saturation is applied (excluding boundary pixels, guard pixels, and light-shielding pixels)
*21: Point defect spanning two or more consecutive pixels

■ Global shutter mode (High-precision mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*22	Vo	0	200	400	DN
Offset variation*23	DSNU	-	15	100	DN rms
Dark output*22	DS	-	10	40	DN/s
Saturation exposure*24	Lsat	-	0.32	-	lx·s
Photosensitivity*24	Sw	6400	8000	-	DN/lx·s
Saturation output*25	Vsat	1600	2300	-	DN
Random noise*22	RN	-	5	8	DN rms
Dynamic range*26	DR	46	53	-	dB
Conversion factor	-	-	37	-	μV/e-
	-	-	0.074	-	DN/e-

■ Rolling shutter mode (High-precision mode)

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*22	Vo	1	0	200	400	DN
		2	0	200	400	
		8	0	200	400	
Offset variation*23	DSNU	1	-	3	10	DN rms
		2	-	3	15	
		8	-	3	15	
Dark output*22	DS	1	-	10	120	DN/s
		2	-	20	240	
		8	-	80	960	
Saturation exposure*24	Lsat	1	-	0.32	-	lx·s
		2	-	0.16	-	
		8	-	0.04	-	
Photosensitivity*24	Sw	1	6400	8000	-	DN/lx·s
		2	12800	16000	-	
		8	51200	64000	-	
Saturation output*25	Vsat	1	3000	3500	-	DN
		2	3000	3500	-	
		8	3000	3500	-	
Random noise*22	RN	1	-	1.7	3.4	DN rms
		2	-	2	4	
		8	-	5.2	8	
Dynamic range*26	DR	1	59	66	-	dB
		2	58	65	-	
		8	51	57	-	
Conversion factor		1	-	37	-	μV/e-
			-	0.12	-	DN/e-
		2	-	74	-	μV/e-
			-	0.24	-	DN/e-
		8	-	280	-	μV/e-
			-	0.96	-	DN/e-

*22: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*23: Standard deviation of output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*24: λ=555 nm
*25: Average of the output values (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels) when light equivalent to twice the saturation exposure is applied but with the offset output subtracted
*26: Ratio of saturation output to random noise
Note: DN (digital number): unit of A/D converter output

■ Global shutter mode (High-speed mode)

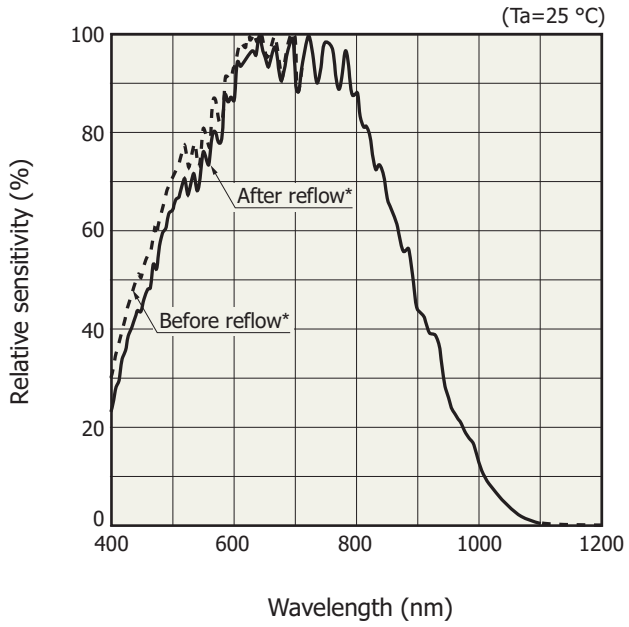
Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*22	Vo	0	200	400	DN
Offset variation*23	DSNU	-	15	100	DN rms
Dark output*22	DS	-	2.5	30	DN/s
Saturation exposure*24	Lsat	-	0.32	-	lx·s
Photosensitivity*24	Sw	1600	2000	-	DN/lx·s
Saturation output*25	Vsat	600	700	-	DN
Random noise*22	RN	-	1.5	2.2	DN rms
Dynamic range*26	DR	49	53	-	dB
Conversion factor	-	-	37	-	μV/e-
	-	-	0.03	-	DN/e-

■ Rolling shutter mode (High-speed mode)

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*22	Vo	1	0	200	400	DN
		2	0	200	400	
		8	0	200	400	
Offset variation*23	DSNU	1	-	3	10	DN rms
		2	-	3	15	
		8	-	3	15	
Dark output*22	DS	1	-	2.5	30	DN/s
		2	-	5	60	
		8	-	20	240	
Saturation exposure*24	Lsat	1	-	0.32	-	lx·s
		2	-	0.16	-	
		8	-	0.04	-	
Photosensitivity*24	Sw	1	1600	2000	-	DN/lx·s
		2	3200	4000	-	
		8	12800	16000	-	
Saturation output*25	Vsat	1	600	700	-	DN
		2	600	700	-	
		8	600	700	-	
Random noise*22	RN	1	-	0.7	1.4	DN rms
		2	-	0.7	1.4	
		8	-	1.4	2.1	
Dynamic range*26	DR	1	53	60	-	dB
		2	53	60	-	
		8	49	54	-	
Conversion factor		1	-	37	-	μV/e-
			-	0.03	-	DN/e-
		2	-	74	-	μV/e-
			-	0.059	-	DN/e-
		8	-	280	-	μV/e-
			-	0.237	-	DN/e-

*22: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*23: Standard deviation of output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*24: λ=555 nm
*25: Average of the output values (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels) when light equivalent to twice the saturation exposure is applied but with the offset output subtracted
*26: Ratio of saturation output to random noise
Note: DN (digital number): unit of A/D converter output

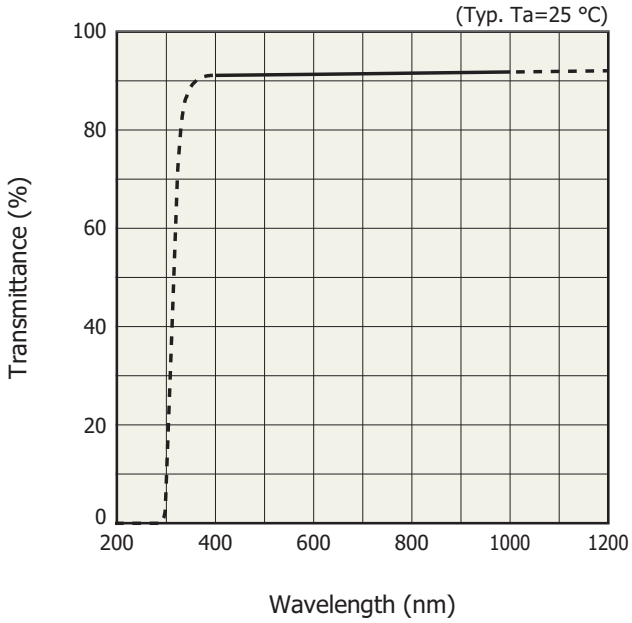
Spectral response (typical example)



* Executed after using the recommended temperature profile for reflow soldering (P11: preheat 100 s, soldering 100 s, peak temperature 260 °C).

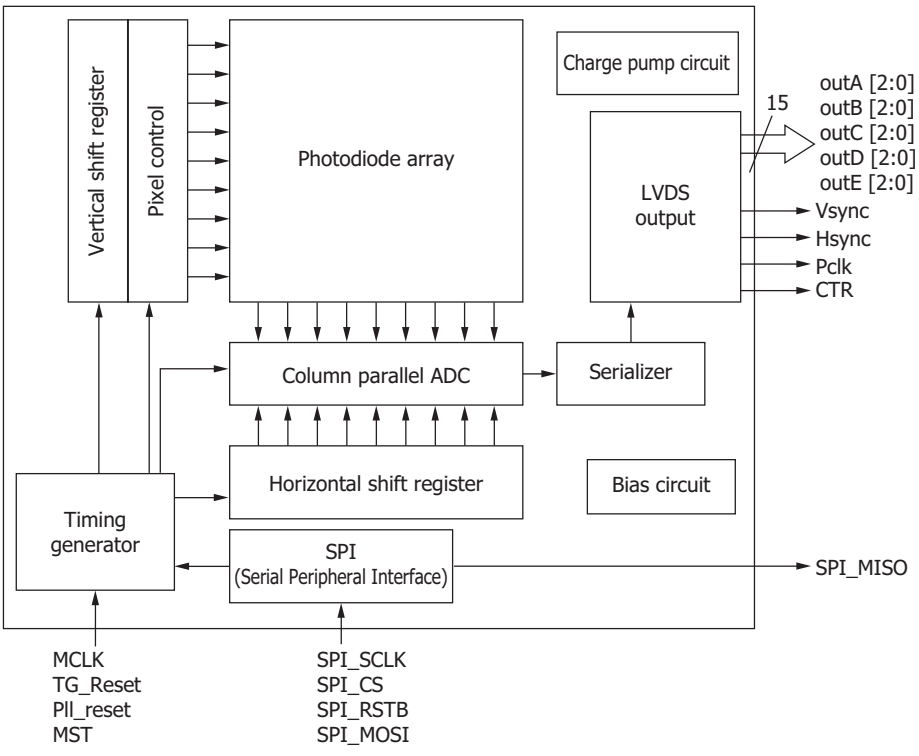
KMPDB0491ED

Spectral transmittance characteristics of window material



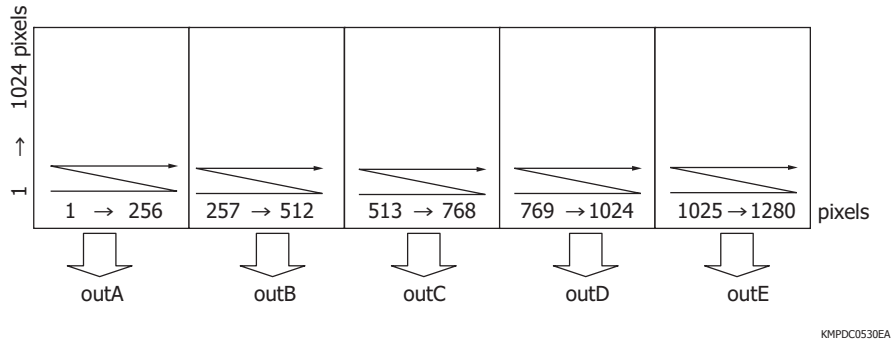
KMPDB0423EA

Block diagram



KMPDC0529EC

Port assignment

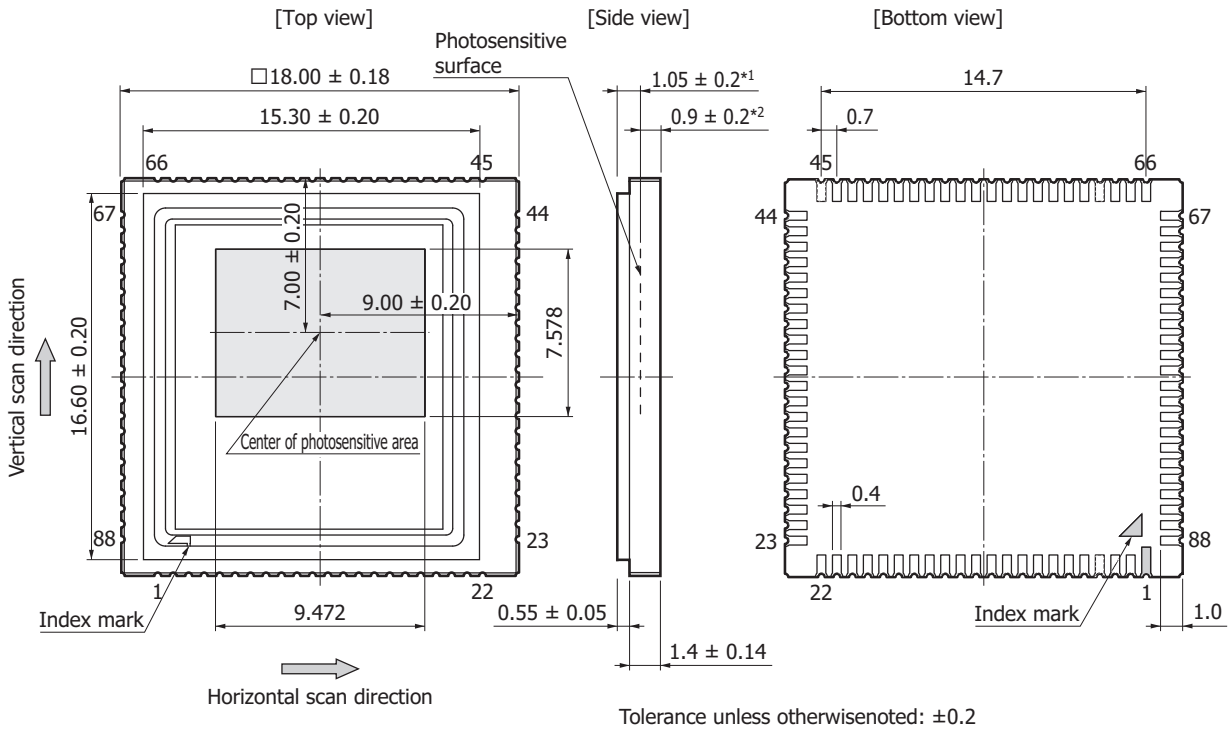


Setup using the SPI and the like

The following parameters can be set using the SPI (serial peripheral interface). However, use MST (external input signal) to set the integration time and blanking period in external start mode.

Parameter	Mode and explanation	
Shutter mode (default: rolling shutter mode)	Rolling shutter mode	Rolling shutter mode is advantageous in that readout noise is small because readout is performed through the CDS circuit. However, the disadvantage is that the integration start/end timing is different for each row.
	Global shutter mode	Global shutter mode is advantageous in that the integration start/end timing is the same for all pixels. However, the disadvantage is that the readout noise is large because a CDS circuit is not used.
Frame start mode (default: internal start pulse mode)	Internal start pulse mode	Readout starts automatically when the power is turned on. The frame period is determined by the number of readout rows and line rate.
	External start pulse mode	Readout starts when the rising edge of MST is detected. MST is also used to control the integration time. The low-level period of MST is roughly the integration time.
Integration time	Internal start pulse mode	Integration time is set using SPI.
	External start pulse mode	Integration time is set using MST.
Blanking period	Internal start pulse mode	Blanking period is set for 0 to 16797215 rows using SPI.
	External start pulse mode	Blanking period is from the end of a readout to the rising edge of the next MST.
Readout region	The readout region can be set at the pixel level. A single readout region can be set in each frame.	
Output gain (rolling shutter mode only)	The gain can be set to 1 time, 2 times, or 8 times.	
Output offset	The output offset value can be adjusted. The default output level is approximately 200 DN.	
Line rate (default: high-precision mode)	High-precision mode	Default line rate, resolution: 12-bit
	High-speed mode	Resolution: 9.4-bit (data width: 10-bit)

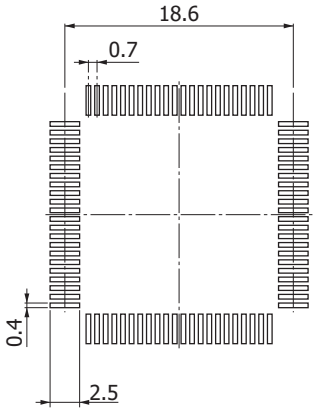
Dimensional outline (unit: mm)



Tolerance unless otherwisenoted: ±0.2
Allgle accuracy of effective pixels: -2°≤θ≤2°
Weight: 1.52 g
*1: Distance from glass surface to photosensitive surface
*2: Distance foem package bottom to photosensitive surface

KMPDA0317EB

Recommended land pattern (unit: mm)



KMPDC0539EA

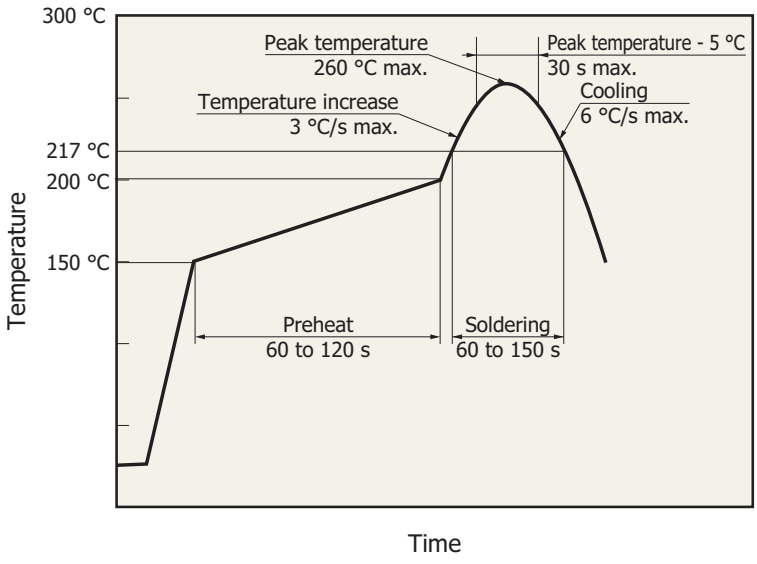
Pin connections

Pin no.	Symbol	Description	I/O
1	Vdd(D)	Digital supply voltage	I
2	GND	Ground	I
3	Vref1*27	Bias voltage for LVDS	O
4	Vref2*27	Bias voltage for LVDS	O
5	Vref3*27	Bias voltage for LVDS	O
6	LVDS_CTR*28	4-bit serializer sync signal	O
7	LVDS_CTRn*28	4-bit serializer sync signal	O
8	LVDS_Vsync*28	Frame (vertical) sync signal	O
9	LVDS_Vsyncn*28	Frame (vertical) sync signal	O
10	LVDS_Hsync*28	Line (horizontal) sync signal	O
11	LVDS_Hsyncn*28	Line (horizontal) sync signal	O
12	LVDS_pclk*28	Pixel sync signal	O
13	LVDS_pclknv*28	Pixel sync signal	O
14	Vdd(C)	Counter supply voltage	I
15	GND	Ground	I
16	Vdd(D)	Digital supply voltage	I
17	GND	Ground	I
18	LVDS_outA[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
19	LVDS_outAn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
20	LVDS_outA[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
21	LVDS_outAn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
22	LVDS_outA[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
23	LVDS_outAn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
24	LVDS_outB[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
25	LVDS_outBn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
26	LVDS_outB[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
27	LVDS_outBn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
28	LVDS_outB[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
29	LVDS_outBn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
30	Vdd(C)	Counter supply voltage	I
31	GND	Ground	I
32	LVDS_outC[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
33	LVDS_outCn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
34	LVDS_outC[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
35	LVDS_outCn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
36	LVDS_outC[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
37	LVDS_outCn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
38	LVDS_outD[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
39	LVDS_outDn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
40	LVDS_outD[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
41	LVDS_outDn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
42	LVDS_outD[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
43	LVDS_outDn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
44	LVDS_outE[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
45	LVDS_outEn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O

Pin no.	Symbol	Description	I/O
46	LVDS_outE[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
47	LVDS_outEn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
48	LVDS_outE[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
49	LVDS_outEn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
50	GND	Ground	I
51	Vdd(D)	Digital supply voltage	I
52	GND	Ground	I
53	Vdd(C)	Counter supply voltage	I
54	GND	Ground	I
55	Vdd(D)	Digital supply voltage	I
56	NC	No connection	-
57	Vref4*27	Bias voltage for amplifier	O
58	Vref5*27	Bias voltage for amplifier	O
59	Vdd(A)	Analog supply voltage	I
60	GND	Ground	I
61	Vdd(A)	Analog supply voltage	I
62	Vdd(A)	Analog supply voltage	I
63	GND	Ground	I
64	Vref_cp2*29	Supply voltage for pixels	I
65	Vref_cp1	Bias voltage for charge pump circuit	I
66	GND	Ground	I
67	Vref6*27	Bias voltage for A/D converter	O
68	Vref7*27	Bias voltage for A/D converter	O
69	Vref8*27	Bias voltage for amplifier	O
70	Vref9*27	Bias voltage for LVDS	O
71	Vref10*27	Bias voltage for amplifier	O
72	NC	No connection	-
73	NC	No connection	-
74	Vref_cp2*29	Supply voltage for pixels	I
75	GND	Ground	I
76	GND	Ground	I
77	GND	Ground	I
78	SPI_MISO	SPI output signal	O
79	MST	Master start signal	I
80	Pll_reset	PLL circuit reset	I
81	SPI_MCLK	Master clock signal (recommended value: 30 MHz)	I
82	TG_RESET	Timing generator circuit reset	I
83	SCLK	SPI clock signal	I
84	SPI_CS	SPI selection signal	I
85	SPI_MOSI	SPI input signal	I
86	SPI_RSTB	SPI reset signal	I
87	Vdd(A)	Analog supply voltage	I
88	GND	Ground	I

*27: A terminal for monitoring the bias voltage generated inside the chip. To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*28: LVDS output. Terminate across the LVDS output wires with a 100 Ω resistor.
*29: Voltage is generated inside the chip, but to improve image quality, supply an external voltage of -1.5 V (that can supply 2 mA).

Recommended temperature profile for reflow soldering (typical example)



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 72 hours.
· The effect that the product is subject to during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

Recommended baking condition

See Precautions (surface mount type products).

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

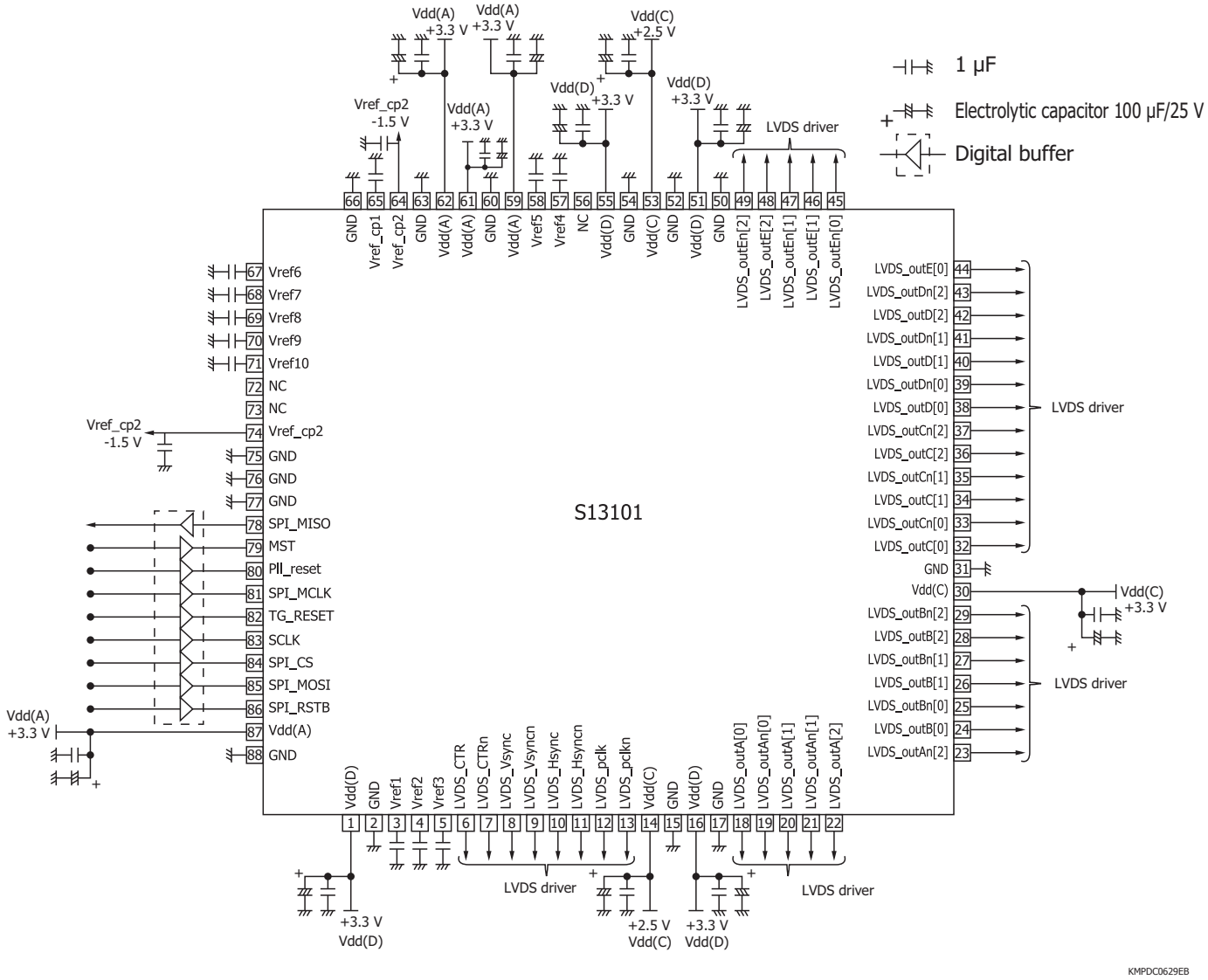
(2) Light input window
If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, a cotton swab, or the like moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no dust or stain remains.

(3) Soldering
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering
Soldering conditions vary depending on the size of the circuit board, reflow oven, and the like. Check the conditions advance before soldering. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

(5) UV light irradiation
This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light to it.

Connection circuit example



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors
· Surface mount type products

■ Technical information
· Image sensors/Terminology

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