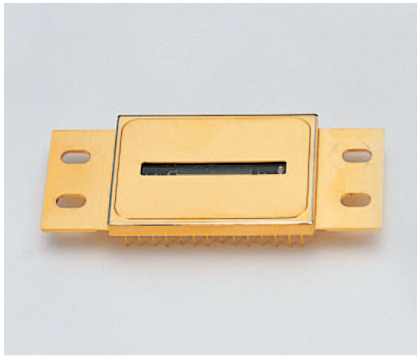


# InGaAs linear image sensor



G14237-512WA

## Near infrared sensors (0.85 to 1.45 $\mu\text{m}$ )

The G14237-512WA is an InGaAs linear image sensor designed for Raman spectroscopy measurement using a 1064 nm laser. Designed specifically for measuring the Raman spectral range, the cutoff wavelength has been reduced from that of the previous product (G11508-512SA) to achieve low dark current. This product consists of an InGaAs photodiode array and CMOS chips made up of charge amplifiers, offset compensation circuit, shift register, and timing generator. The charge amplifiers consist of CMOS transistor arrays and are connected to each pixel of the InGaAs photodiode array. The signal from each pixel is read out in charge integration mode, which provides high sensitivity and stable operation in the near infrared region. The package is hermetically sealed for excellent reliability.

The signal processing circuit on the CMOS chip can be set to one of four conversion efficiency (CE) settings using an external voltage.

### Features

- **Low noise, extremely low dark current [1/10 or less than that of the previous product (cutoff wavelength: 1.7  $\mu\text{m}$ )]**
- **Selectable from four conversion efficiency types**
- **Built-in saturation countermeasure circuit**
- **Built-in CDS circuit\*<sup>1</sup>**
- **Built-in thermistor**
- **Easy operation (built-in timing generator\*<sup>2</sup>)**
- **High resolution: 25  $\mu\text{m}$  pitch**

### Applications

- **Raman spectroscopy measurement (using a 1064 nm laser) and the like**

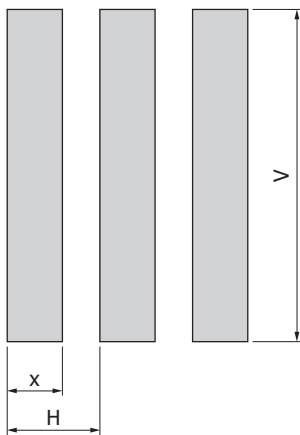
\*1: On charge amplifiers, the reset noise that occurs when the integration capacitance is reset is dominant. However, the CDS circuit, which takes the difference between the signal after the completion of the integration time and the signal immediately after resetting, greatly reduces the reset noise.

\*2: Previously, multiple timing signals were applied using external PLDs or the like to run the shift register. This image sensor has a built-in CMOS circuit for timing generation. All timing signals are generated inside the image sensor by simply applying CLK and Reset signals.

**Structure**

Type no.	Specification	Unit
Cooling	Two-stage TE-cooled	-
Image size	12.8 × 0.5	mm
Pixel size	25 (H) × 500 (V)	μm
Pixel pitch	25	μm
Total number of pixels	512	pixels
Number of effective pixels	512	pixels
Fill factor	100	%
Package	28-pin metal (refer to dimensional outline)	-
Window material	Sapphire (with anti-reflective coating)	-
Dedicated driver circuit	-	-

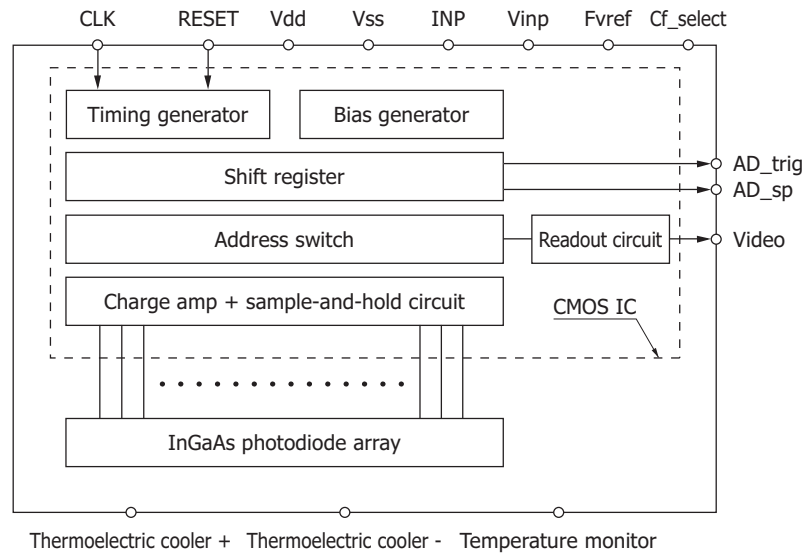
**Enlarged view of photosensitive area**



Number of pixels	x	H	V
512	10	25	500

KMIRC0112EA

**Block diagram**



KMIRC0103EA

**Absolute maximum ratings**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vdd, INP, Fvref Vinp, PDN	Ta=25 °C	-0.3	-	+6	V
Clock pulse voltage	Vclk	Ta=25 °C	-0.3	-	+6	V
Reset pulse voltage	V(res)	Ta=25 °C	-0.3	-	+6	V
Gain selection terminal voltage	Vcf sel	Ta=25 °C	-0.3	-	+6	V
Operating temperature	Topr	No dew condensation*3	-20	-	+70	°C
Storage temperature	Tstg	No dew condensation*3	-40	-	+85	°C
Soldering conditions	-		Up to 260 °C, up to 10 s			-
Thermistor power dissipation	Pd_th	Ta=25 °C	-	-	400	mW

\*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Absolute maximum ratings indicate values that must not be exceeded. Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

### Recommended terminal voltage (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vdd	4.7	5.0	5.3	V
Differential reference voltage	Fvref	1.1	1.2	1.3	V
Video line reset voltage	Vinp	3.9	4.0	4.1	V
Input stage amplifier reference voltage	INP	3.9	4.0	4.1	V
Photodiode cathode voltage	PDN	3.9	4.0	4.1	V
Ground	Vss	-	0	-	V
Clock pulse voltage	High	4.7	5.0	5.3	V
	Low	0	0	0.4	
Reset pulse voltage	High	4.7	5.0	5.3	V
	Low	0	0	0.3	

### Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Current consumption	I(Vdd)	-	85	120	mA
	Ifvref	-	-	1	
	Ivinp	-	-	1	
	Iinp	-	-	1	
	Ipdn	-	-	1	
Clock frequency	fop	0.1	1	5	MHz
Video data rate	DR	0.1	fop	5	MHz
Video output voltage	High	VH	-	4.0	V
	Low	VL	-	1.2	
Output offset voltage	Vos	-	Fvref	-	V
Output impedance	Zo	-	5	-	kΩ
AD_trig, AD_sp Pulse voltage	High	Vtrig, Vsp	-	Vdd	V
	Low		-	GND	
Thermistor resistance	Rth	9.0	10.0	11.0	kΩ
Thermistor B constant*4	B	-	3950	-	K

\*4: T<sub>1</sub>=25 °C, T<sub>2</sub>=50 °C

### Electrical and optical characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fref=1.2 V, Vclk=5 V, fop=1 MHz, CE=16 nV/e<sup>-</sup>)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range	λ		-	0.85 to 1.45	-	μm
Peak sensitivity wavelength	λp		1.25	1.35	1.45	μm
Photosensitivity	S	λ=λp	0.8	0.9	-	A/W
Conversion efficiency*5	CE	Cf=10 pF	-	16	-	nV/e <sup>-</sup>
		Cf=1 pF	-	160	-	
		Cf=0.5 pF	-	320	-	
		Cf=0.17 pF	-	930	-	
Photoresponse nonuniformity*6	PRNU		-	±3	±5	%
Saturation output voltage	Vsat		2.7	2.8	-	V
Full well capacity	Csat	CE=16 nV/e <sup>-</sup>	-	175	-	Me <sup>-</sup>
		CE=160 nV/e <sup>-</sup>	-	17.5	-	
		CE=320 nV/e <sup>-</sup>	-	8.75	-	
		CE=930 nV/e <sup>-</sup>	-	3.0	-	
Dark output	VD	CE=16 nV/e <sup>-</sup>	-0.2	±0.01	0.2	V/s
Dark current	ID	CE=16 nV/e <sup>-</sup>	-2	±0.1	2	pA
Readout noise*7	Nread	CE=16 nV/e <sup>-</sup>	-	200	400	μV rms
		CE=160 nV/e <sup>-</sup>	-	300	500	
Dynamic range	Drange	CE=16 nV/e <sup>-</sup>	6750	14000	-	-
Defect pixels*8	-	CE=16 nV/e <sup>-</sup>	-	-	1	%

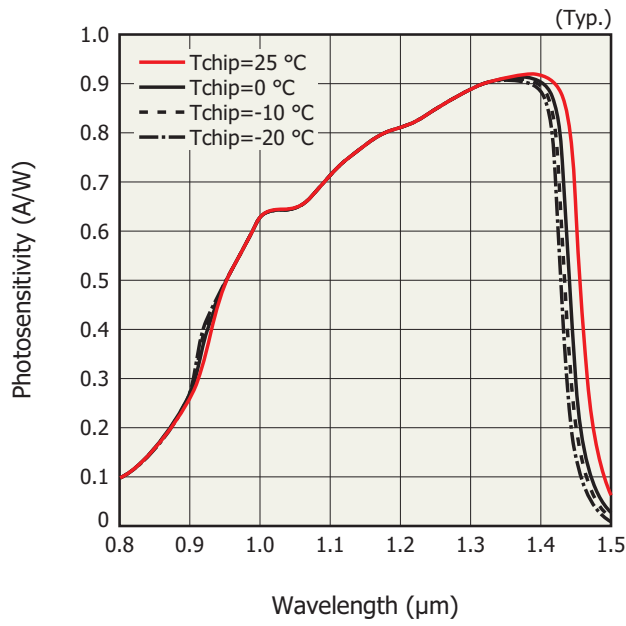
\*5: For switching the conversion efficiency, see the pin connections.

\*6: Measured at approximately 50% saturation and 10 ms integration time, pixel deviation after subtracting the dark output, excluding the first and last pixels

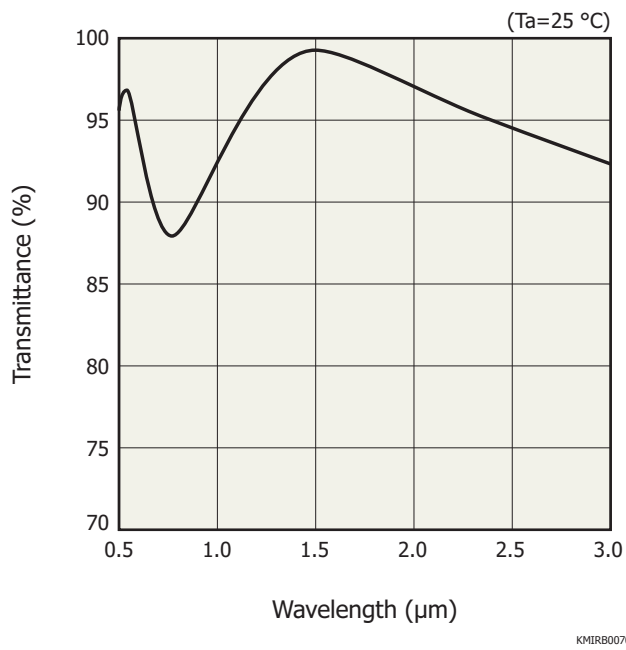
\*7: Integration time when CE=16 nV/e<sup>-</sup> is 10 ms. Integration time when CE=160 nV/e<sup>-</sup> is 1 ms.

\*8: Pixels whose photoresponse nonuniformity, readout noise, or dark current is outside the specifications

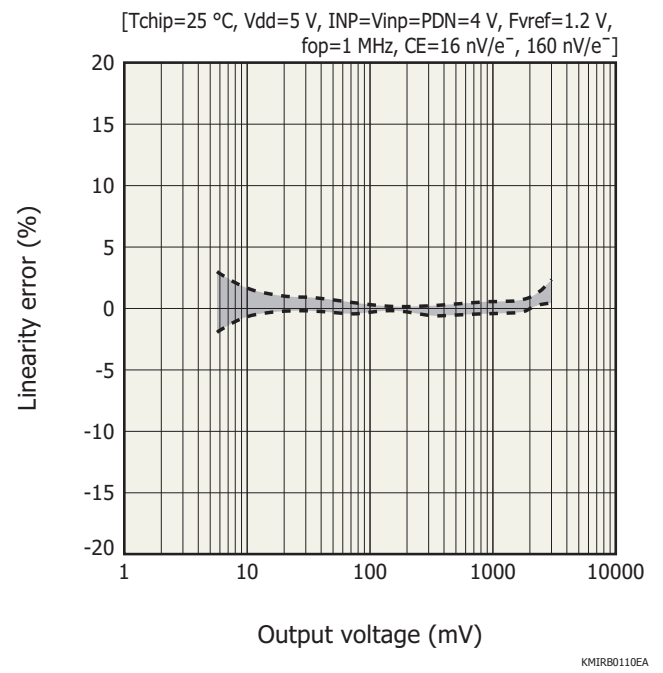
**Spectral response**



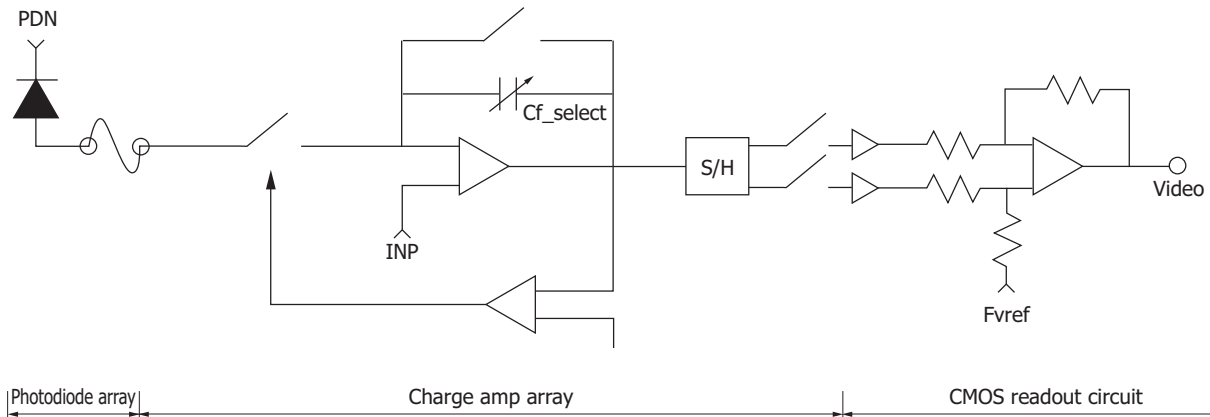
**Spectral transmittance characteristics of window material (typical example)**



**Linearity error (typical example)**

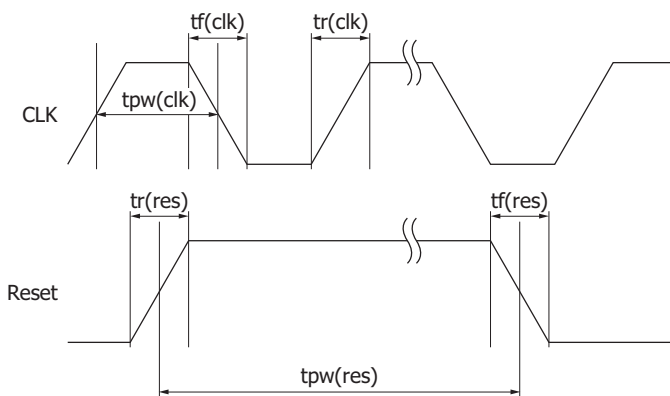
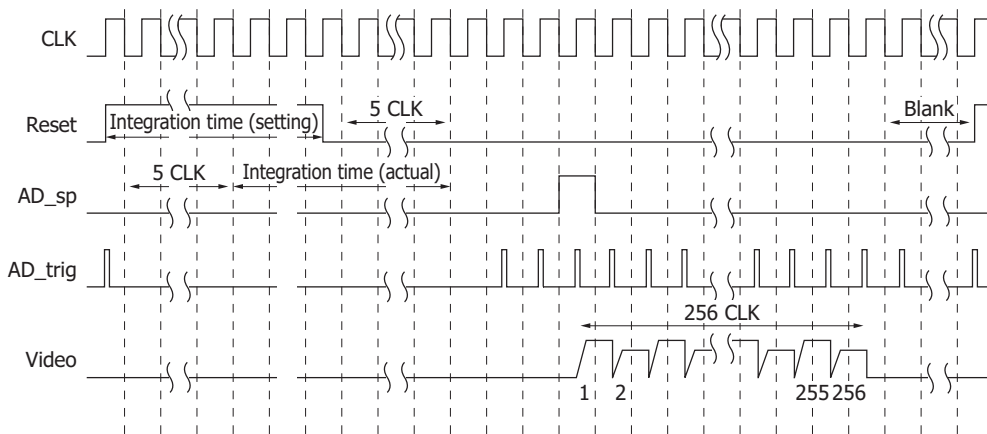


**Equivalent circuit**



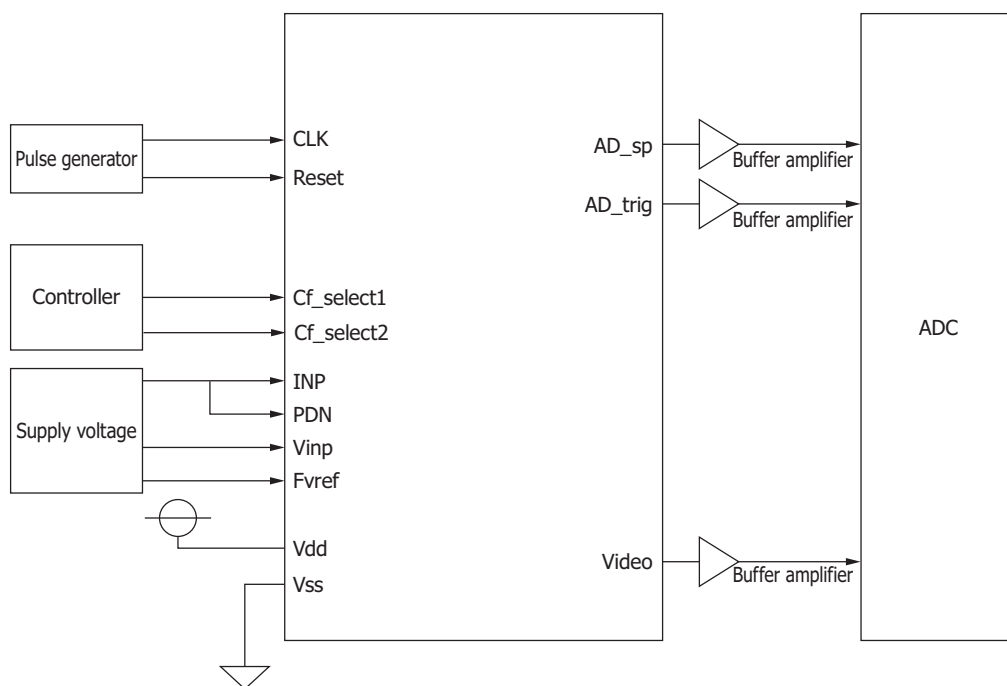
KMIRC0049EA

**Timing chart (each video line)**



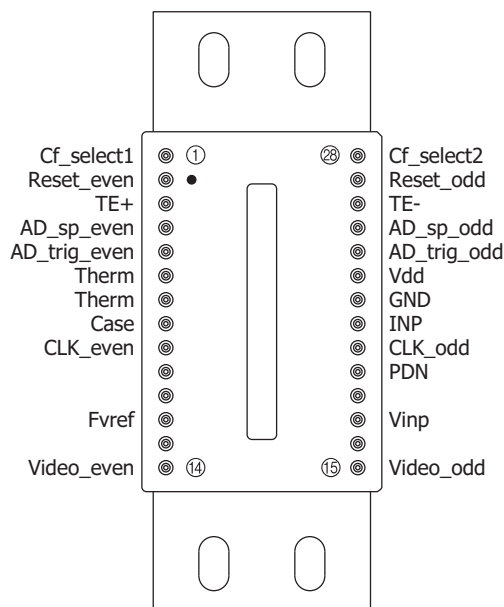
KMIRC0104EA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	fop	0.1	1	5	MHz
Clock pulse width	tpw(clk)	60	500	5000	ns
Clock pulse rise/fall times	tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	tpw(res)	High	-	-	clocks
		Low	284	-	
Reset pulse rise/fall times	tr(res), tf(res)	0	20	30	ns

**Connection example**

KMRC0056EB

### Pin connections (top view)



KMIRC0113EA

Terminal name	Input/output	Function and recommended connection	Note
PDN	Input	InGaAs photodiode's cathode bias terminal Set to the same potential as INP.	4.0 V
AD_sp	Output	Digital start signal for A/D conversion	0 to 5 V
Cf_select1, 2	Input*9	Signal for selecting the feedback capacitance (integration capacitance) on the CMOS chip	0 V or 5 V
Therm	Output	Thermistor for monitoring the temperature inside the package	-
AD_trig	Output	Sampling sync signal for A/D conversion	0 to 5 V
Reset	Input	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. Integration time is determined by the high level period of this pulse.	0 to 5 V
CLK	Input	Clock pulse for operating the CMOS shift register	0 to 5 V
INP	Input	Input stage amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip. Set to the same potential as PDN.	4.0 V
Vinp	Input	Video line reset voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	4.0 V
Fvref	Input	Differential amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	1.2 V
Video	Output	Differential amplifier output. This is an analog video signal.	1.2 to 4.0 V
Vdd	Input	Supply voltage (+5 V) for operating the signal processing circuit on the CMOS chip	5 V
GND	Input	Ground for the signal processing circuit on the CMOS chip (0 V)	0 V
Case	-	This terminal is connected to the package.	-
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler for cooling the photodiode array	-

\*9: The conversion efficiency is determined by the supply voltage to the Cf\_select terminal as follows.

Conversion efficiency	Cf_select1	Cf_select2
16 nV/e <sup>-</sup>	High	High
160 nV/e <sup>-</sup>	High	Low
320 nV/e <sup>-</sup>	Low	High
930 nV/e <sup>-</sup>	Low	Low

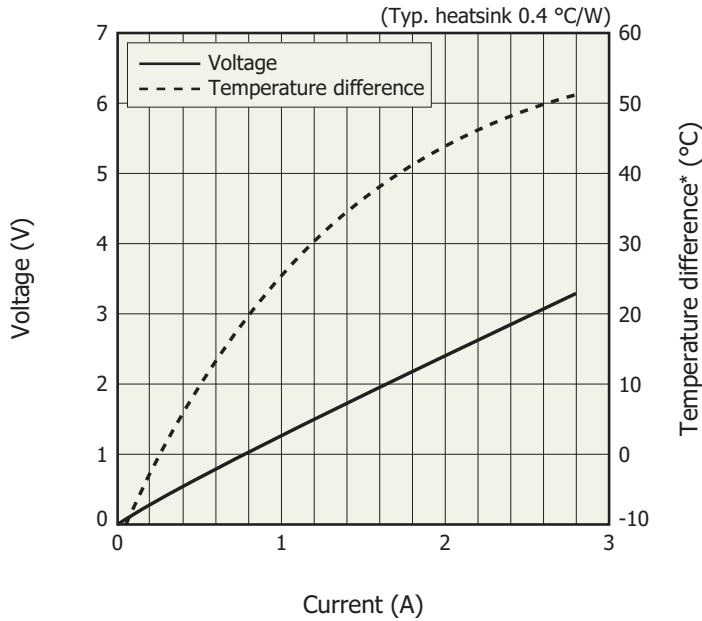
Low: 0 V (GND), High: 5 V (Vdd)

**TE-cooler specifications (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vclk=5 V, fop=1 MHz)**

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Allowable TE-cooler current		Ic max.	-	-	2.8	A
Allowable TE-cooler voltage		Vc max.	-	-	4.0	V
Temperature difference*10	Ic=2.6 A	$\Delta T$	50	-	-	°C
Thermistor resistance		Rth	9	10	11	k $\Omega$
Thermistor power dissipation		Pth	-	-	400	mW

\*10: Temperature difference between the photosensitive area and package heat dissipation area

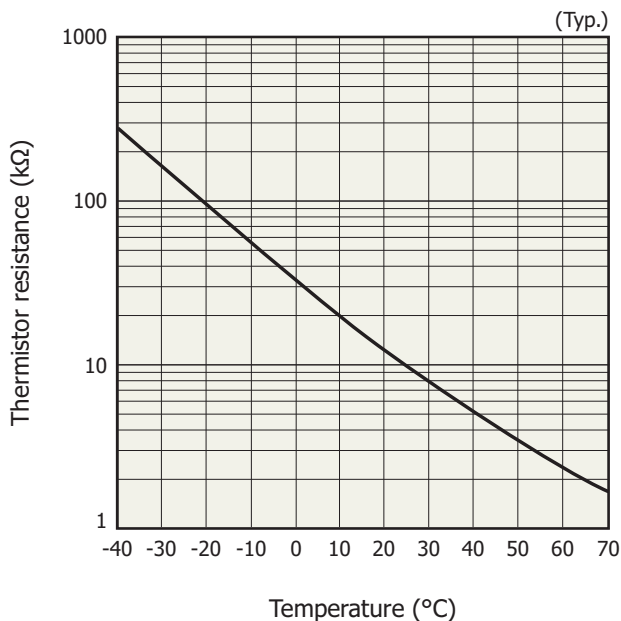
**TE-cooler temperature characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vclk=5 V, fop=1 MHz)**



\* Temperature difference between the photosensitive area and package heat dissipation area

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**Thermistor temperature characteristics**

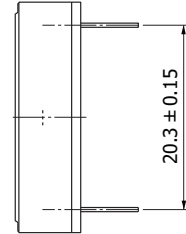
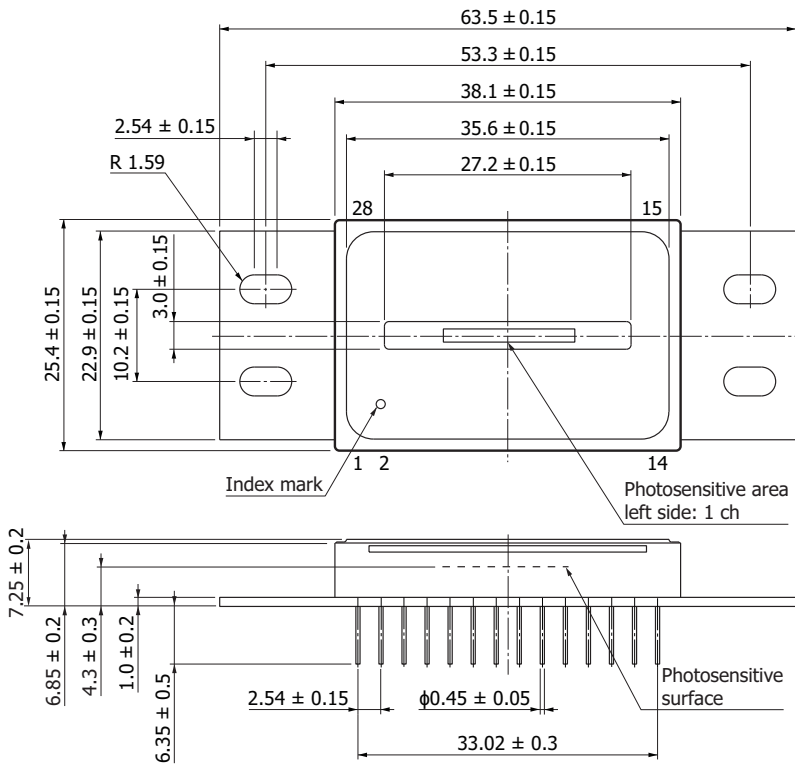


Temperature (°C)	Thermistor resistance (k $\Omega$ )	Temperature (°C)	Thermistor resistance (k $\Omega$ )
-40	281	20	12.5
-35	208	25	10.0
-30	155	30	8.06
-25	117	35	6.53
-20	88.8	40	5.32
-15	68.4	45	4.36
-10	53.0	50	3.59
-5	41.2	55	2.97
0	32.1	60	2.47
5	25.1	65	2.07
10	19.8	70	1.74
15	15.7		

KMIRB0061EA



**Dimensional outline (unit: mm)**



Center accuracy of photosensitive area:  $\pm 0.3$  or less  
 (with respect to package center)  
 Rotation accuracy of photosensitive area  $\pm 2^\circ$  or less  
 (with respect to package center)  
 Chip material: InGaAs  
 Package material: FeNi alloy  
 Lead processing: Ni/Au plating  
 Lead material: FeNiCo alloy  
 Window material: Sapphire  
 Window refractive index: 1.76  
 Window thickness: 0.66  
 AR coating: Available (1.55  $\mu\text{m}$  peak)  
 Window sealing method: Brazing  
 Cap sealing: Welding

KMIRA0038EA

## Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

## Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

### ■ Precautions

- Disclaimer
- Safety precautions
- Image sensors

Information described in this material is current as of December 2017.

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