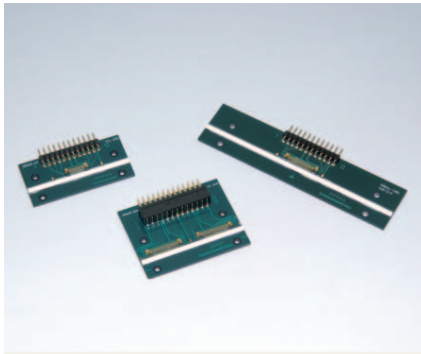


Photodiode arrays with amplifier



S8865-64G/-128G/-256G
S8866-64G-02/-128G-02

Photodiode array combined with signal processing IC for X-ray detection

The S8866-64G-02/-128G-02 are photodiode arrays with an amplifier and a phosphor sheet attached to the photosensitive area for X-ray detection. The signal processing circuit chip is formed by CMOS process and incorporates a timing generator, shift register, charge amplifier array, clamp circuit and hold circuit, making the external circuit configuration simple. A long, narrow image sensor can be configured by arranging multiple arrays in a row. As the dedicated driver circuit, the C9118 series (sold separately) is provided. (Not compatible with the S8865-256G and S8866-64G-02.)

Features

- Large element pitch: 5 types available
S8865-64G: 0.8 mm pitch × 64 ch
S8865-128G: 0.4 mm pitch × 128 ch
S8865-256G: 0.2 mm pitch × 256 ch
S8866-64G-02: 1.6 mm pitch × 64 ch
S8866-128G-02: 0.8 mm pitch × 128 ch
- 5 V power supply operation
- Simultaneous integration by using a charge amplifier array
- Sequential readout with a shift register (Data rate: 500 kHz max.)
- Low dark current due to zero-bias photodiode operation
- Integrated clamp circuit allows low noise and wide dynamic range
- Integrated timing generator allows operation at two different pulse timings
- Detectable energy range: 30 k to 100 keV

Applications

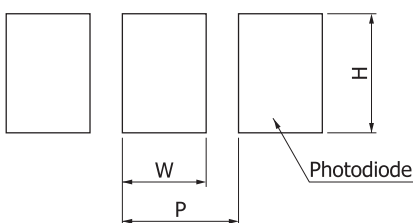
- Line sensors for X-ray detection

Structure

| Parameter | Symbol*1 | S8865-64G | S8865-128G | S8865-256G | S8866-64G-02 | S8866-128G-02 | Unit |
|--------------------------------------|----------|-------------|------------|------------|--------------|---------------|------|
| Element pitch | P | 0.8 | 0.4 | 0.2 | 1.6 | 0.8 | mm |
| Element diffusion width | W | 0.7 | 0.3 | 0.1 | 1.5 | 0.7 | mm |
| Element height | H | 0.8 | 0.6 | 0.3 | 1.6 | 0.8 | mm |
| Number of elements | - | 64 | 128 | 256 | 64 | 128 | - |
| Effective photosensitive area length | - | 51.2 | 51.2 | 51.2 | 102.4 | 102.4 | mm |
| Board material | - | Glass epoxy | | | | | - |

*1: Refer to following figure.

Enlarged drawing of photosensitive area



KMPDC0072EA

▣ Absolute maximum ratings

| Parameter | Symbol | Value | Unit |
|---------------------------------|-----------|------------|------|
| Supply voltage | Vdd | -0.3 to +6 | V |
| Reference voltage | Vref | -0.3 to +6 | V |
| Photodiode voltage | Vpd | -0.3 to +6 | V |
| Gain selection terminal voltage | Vgain | -0.3 to +6 | V |
| Master/slave selection voltage | Vms | -0.3 to +6 | V |
| Clock pulse voltage | V (CLK) | -0.3 to +6 | V |
| Reset pulse voltage | V (RESET) | -0.3 to +6 | V |
| External start pulse voltage | V (EXTSP) | -0.3 to +6 | V |
| Operating temperature*2 | Topr | -5 to +60 | °C |
| Storage temperature*2 | Tstg | -10 to +70 | °C |

*2: No dew condensation

When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Recommended terminal voltage

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------|------------|------|------------|------|
| Supply voltage | Vdd | 4.75 | 5 | 5.25 | V |
| Reference voltage | Vref | 4 | 4.5 | 4.6 | V |
| Photodiode voltage | Vpd | - | Vref | - | V |
| Gain selection terminal voltage | High gain | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low gain | 0 | - | 0.4 | V |
| Master/slave selection voltage | High level*3 | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level*4 | 0 | - | 0.4 | V |
| Clock pulse voltage | High level | 3.3 | Vdd | Vdd + 0.25 | V |
| | Low level | 0 | - | 0.4 | V |
| Reset pulse voltage | High level | 3.3 | Vdd | Vdd + 0.25 | V |
| | Low level | 0 | - | 0.4 | V |
| External start pulse voltage | High level | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low level | 0 | - | 0.4 | V |

*3: Parallel

*4: Serial at 2nd or later stages

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|---------------------------|------|------|------|---------|
| Clock pulse frequency*5 | f(CLK) | 40 | - | 2000 | kHz |
| Line rate | S8865-64G | - | 7339 | - | Lines/s |
| | S8865-128G, S8866-128-02G | - | 3784 | - | |
| | S8865-256G | - | 1922 | - | |
| | S8866-64G-02 | - | 6838 | - | |
| Output impedance | Zo | - | 3 | - | kΩ |
| Power consumption | S8865-64G, S8866-64G-02 | - | 100 | - | mW |
| | S8865-128G, S8866-128G-02 | - | 180 | - | |
| | S8865-256G | - | 360 | - | |
| Charge amp feedback capacitance | High gain | - | 0.5 | - | pF |
| | Low gain | - | 1 | - | |

* 5: Video data rate is 1/4 of clock pulse frequency f(CLK).

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(RESET)=5 V, Vgain=5 V (High gain), 0 V (Low gain)]

S8865-64G/-128G/-256G

| Parameter | Symbol | S8865-64G | | | S8865-128G | | | S8865-256G | | | Unit |
|-------------------------------|--|-----------|-------|----------|------------|-------|----------|------------|-------|----------|----------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Peak sensitivity wavelength*6 | λ_p | - | 720 | - | - | 720 | - | - | 720 | - | nm |
| Dark output voltage*7 | High gain | - | 0.01 | 0.2 | - | 0.01 | 0.2 | - | 0.01 | 0.2 | mV |
| | Low gain | - | 0.005 | 0.1 | - | 0.005 | 0.1 | - | 0.005 | 0.1 | |
| Saturation output voltage | Vsat | 3.0 | 3.5 | - | 3.0 | 3.5 | - | 3.0 | 3.5 | - | V |
| Saturation exposure*6 *8 | High gain | - | 0.8 | 1.0 | - | 2.4 | 3.0 | - | 15 | 19 | m/lx · s |
| | Low gain | - | 1.6 | 2.0 | - | 4.8 | 6.0 | - | 30 | 37.5 | |
| Photosensitivity*6 *8 | High gain | 3520 | 4400 | - | 1200 | 1500 | - | 200 | 250 | - | V/lx · s |
| | Low gain | 1760 | 2200 | - | 600 | 750 | - | 100 | 125 | - | |
| Photoresponse nonuniformity*9 | 3 channels from both ends | - | - | -35, +10 | - | - | -55, +10 | - | - | -70, +10 | % |
| | All channels excluding 3 channels from both ends | - | - | ±10 | - | - | ±10 | - | - | ±10 | |
| Noise*10 | High gain | - | 1.3 | 2.0 | - | 1.0 | 1.5 | - | 0.8 | 1.2 | mV rms |
| | Low gain | - | 0.7 | 1.1 | - | 0.6 | 0.9 | - | 0.5 | 0.75 | |
| Output offset voltage*11 | Vos | - | Vref | - | - | Vref | - | - | Vref | - | V |

S8866-64G-02/-128G-02

| Parameter | Symbol | S8866-64G-02 | | | S8866-128G-02 | | | Unit |
|-------------------------------|--|--------------|-------|----------|---------------|-------|----------|----------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Peak sensitivity wavelength*6 | λ_p | - | 720 | - | - | 720 | - | nm |
| Dark output voltage*7 | High gain | - | 0.01 | 0.2 | - | 0.01 | 0.2 | mV |
| | Low gain | - | 0.005 | 0.1 | - | 0.005 | 0.1 | |
| Saturation output voltage | Vsat | 3 | 3.5 | - | 3 | 3.5 | - | V |
| Saturation exposure*6 *8 | High gain | - | 0.2 | 0.25 | - | 0.8 | 1.0 | m/lx · s |
| | Low gain | - | 0.4 | 0.5 | - | 1.6 | 2.0 | |
| Photosensitivity*6 *8 | High gain | 14400 | 18000 | - | 3520 | 4400 | - | V/lx · s |
| | Low gain | 7200 | 9000 | - | 1760 | 2200 | - | |
| Photoresponse nonuniformity*9 | 3 channels from both ends | - | - | -25, +10 | - | - | -35, +10 | % |
| | All channels excluding 3 channels from both ends | - | - | ±10 | - | - | ±10 | |
| Noise*10 | High gain | - | 2.0 | 3.0 | - | 1.3 | 2.0 | mVrms |
| | Low gain | - | 1.1 | 1.7 | - | 0.7 | 1.1 | |
| Output offset voltage*11 | Vos | - | Vref | - | - | Vref | - | V |

*6: Measured without phosphor sheet

*7: Integration time $t_s=1$ ms

*8: Measured with a 2856 K tungsten lamp

*9: When the photodiode array is exposed to uniform light which is 50% of the saturation exposure, the photoresponse nonuniformity (PRNU) is defined as follows:

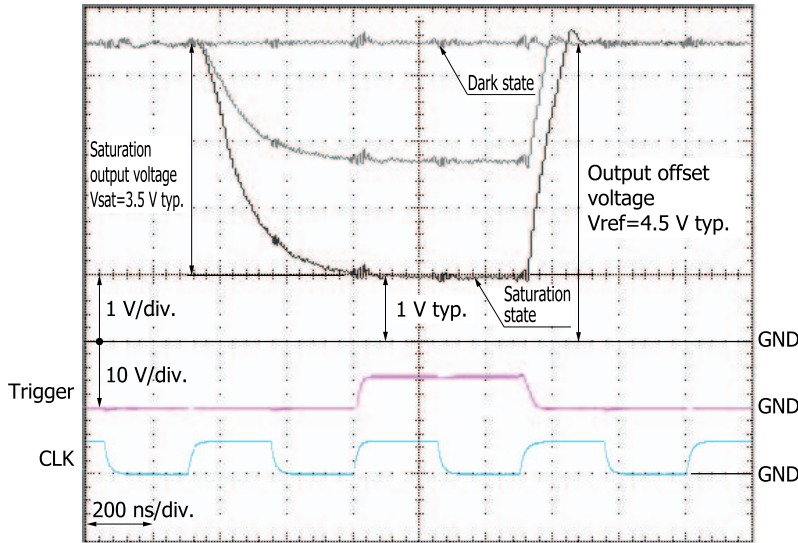
$$PRNU = \Delta X / X \times 100 [\%]$$

X: average output of all elements, ΔX : difference between X and the maximum or minimum output, whichever is larger.

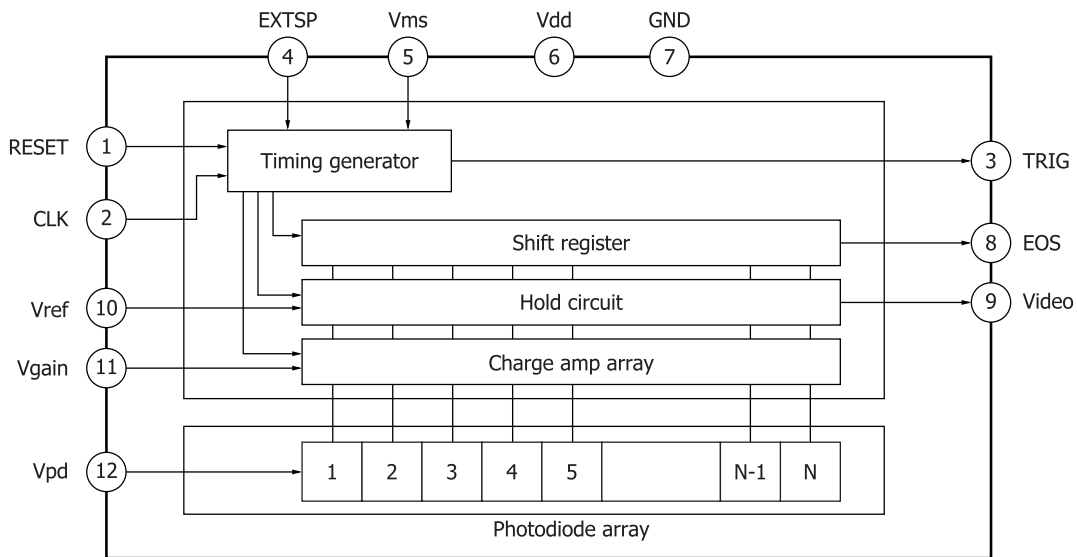
*10: Measured with a video data rate of 50 kHz and $t_s=1$ ms in dark state

*11: Video output is negative-going output with respect to the output offset voltage.

Output waveform of one element



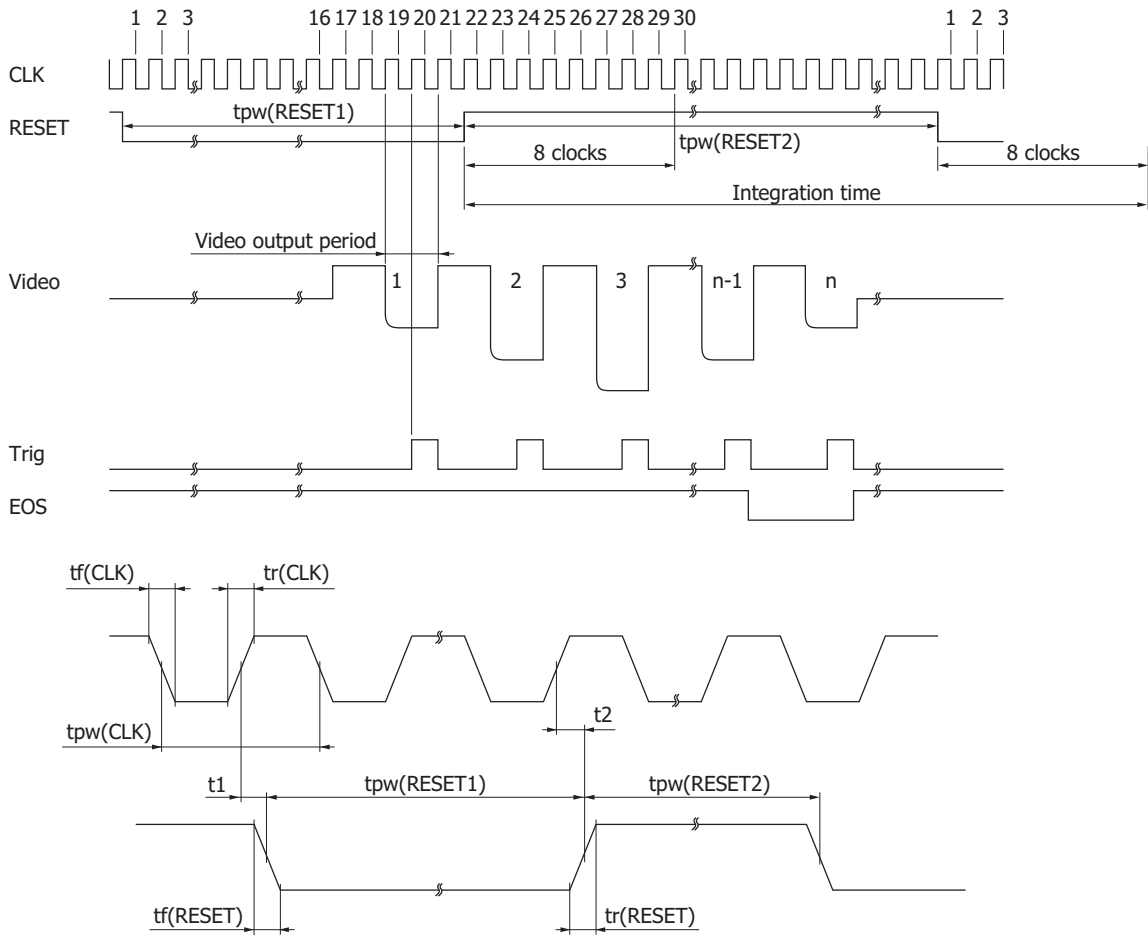
Block diagram



KMPDC0153EA

Timing chart

S8865-64G/-128G/-256G, S8866-128G-02



KMPDC0289EC

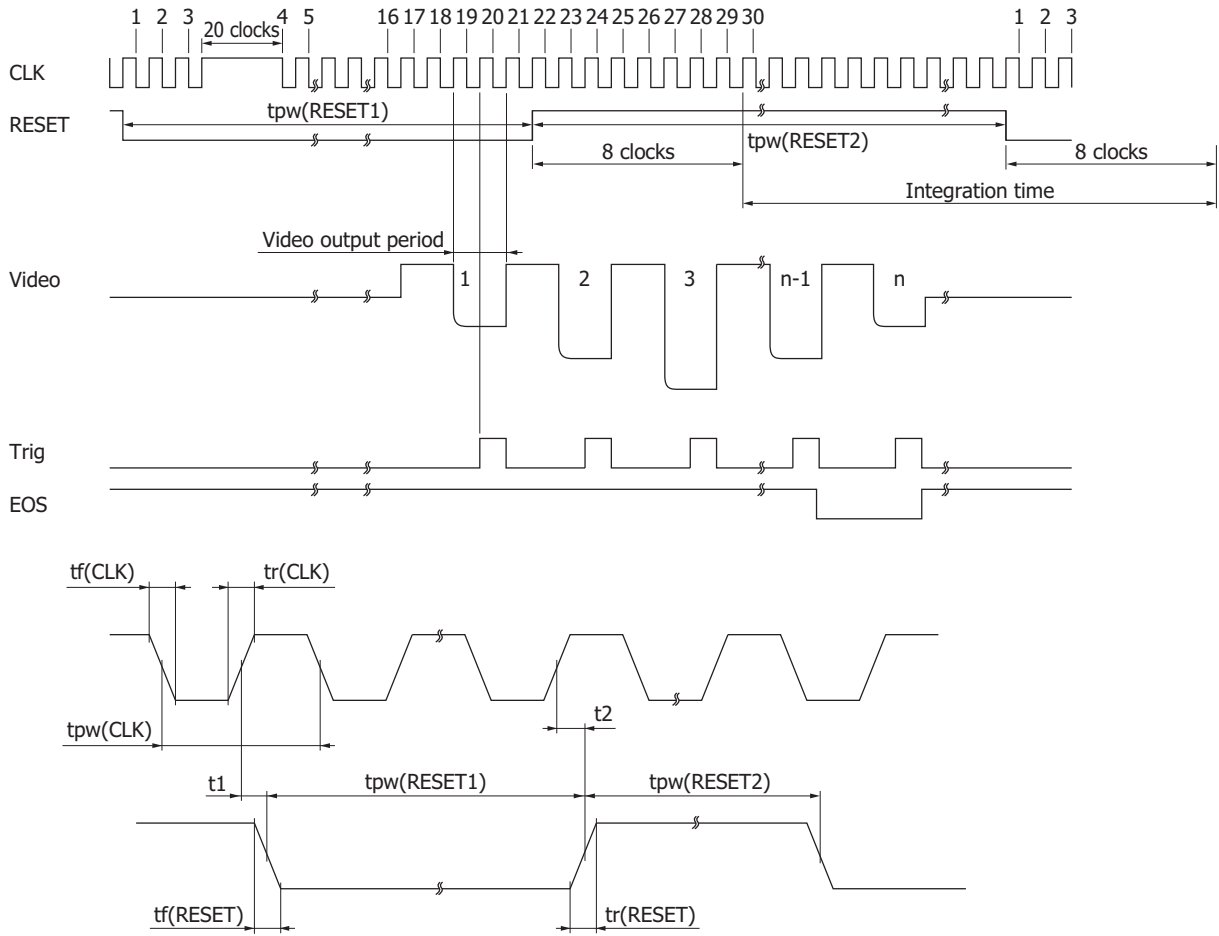
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------------|------|------|-------|------|
| Clock pulse width | tpw(CLK) | 500 | - | 25000 | ns |
| Clock pulse rise/fall times | tr(CLK), tf(CLK) | 0 | 20 | 30 | ns |
| Reset pulse width 1 | tpw(RESET1) | 21 | - | - | CLK |
| Reset pulse width 2 | tpw(RESET2) | 20 | - | - | CLK |
| Reset pulse rise/fall times | tr(RESET), tf(RESET) | 0 | 20 | 30 | ns |
| Clock pulse-reset pulse timing 1 | t1 | -20 | 0 | 20 | ns |
| Clock pulse-reset pulse timing 2 | t2 | -20 | 0 | 20 | ns |

1. The internal timing circuit starts operation at the falling edge of CLK immediately after a RESET pulse goes Low.
2. When the falling edge of each CLK is counted as "1 clock", the video signal of the 1st channel appears between "18.5 clocks and 20.5 clocks". Subsequent video signals appear every 4 clocks.
3. The trigger pulse for the 1st channel rises at a timing of 19.5 clocks and then rises every 4 clocks. The rising edge of each trigger pulse is the recommended timing for data acquisition.
4. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse.

After the RESET pulse next changes from High to Low, signals integrated within this period are sequentially read out as time-series signals by the shift register operation. The rise and fall of a RESET pulse must be synchronized with the rise of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "16.5 + 4 × N (number of elements)" clocks.

5. The video signal after an EOS signal output becomes a high impedance state, and the video output will be indefinite.

S8866-64G-02

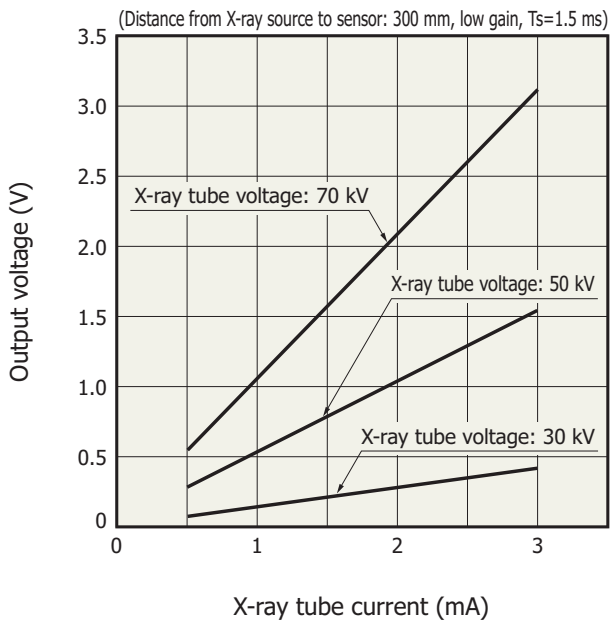


KMPDC0278EC

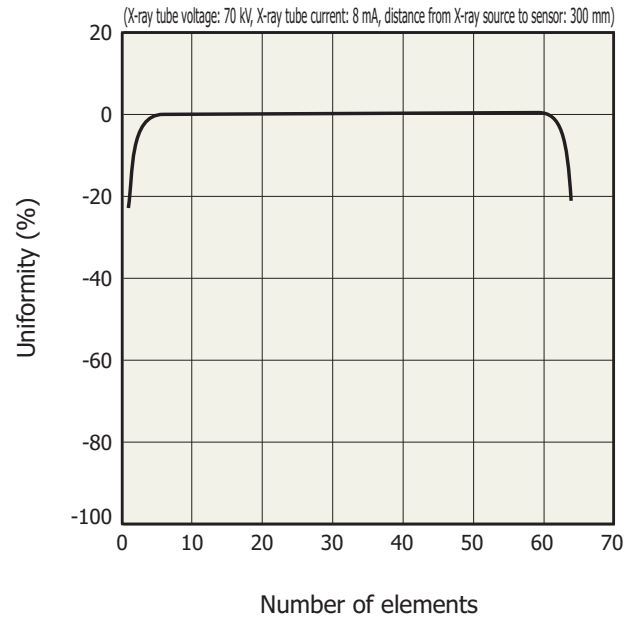
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|------------------------|------|------|-------|------|
| Clock pulse width | tpw (CLK1), tpw (CLK2) | 500 | - | 12500 | ns |
| Clock pulse rise/fall times | tr (CLK), tf (CLK) | 0 | 20 | 30 | ns |
| Reset pulse width 1 | tpw (RESET1) | 21 | - | - | CLK |
| Reset pulse width 2 | tpw (RESET2) | 20 | - | - | CLK |
| Reset pulse rise/fall times | tr (RESET), tf (RESET) | 0 | 20 | 30 | ns |
| Clock pulse-reset pulse timing 1 | t1 | -20 | 0 | 20 | ns |
| Clock pulse-reset pulse timing 2 | t2 | -20 | 0 | 20 | ns |

1. The internal timing circuit starts operation at the falling edge of CLK immediately after a RESET pulse goes Low.
2. When the falling edge of each CLK is counted as "1 clock", the video signal of the 1st channel appears between "18.5 clocks and 20.5 clocks". Subsequent video signals appear every 4 clocks.
3. To obtain video signals, extend the High period 3 clocks from the falling edge of CLK immediately after the RESET pulse goes Low, to a 20 clock period.
4. The trigger pulse for the 1st channel rises at a timing of 19.5 clocks and then rises every 4 clocks. The rising edge of each trigger pulse is the recommended timing for data acquisition.
5. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse. After the RESET pulse next changes from High to Low, signals integrated within this period are sequentially read out as time-series signals by the shift register operation. The rise and fall of a RESET pulse must be synchronized with the rise of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "36.5 + 4 × N (number of elements)" clocks.
6. The video signal after an EOS signal output becomes a high impedance state, and the video output will be indefinite.

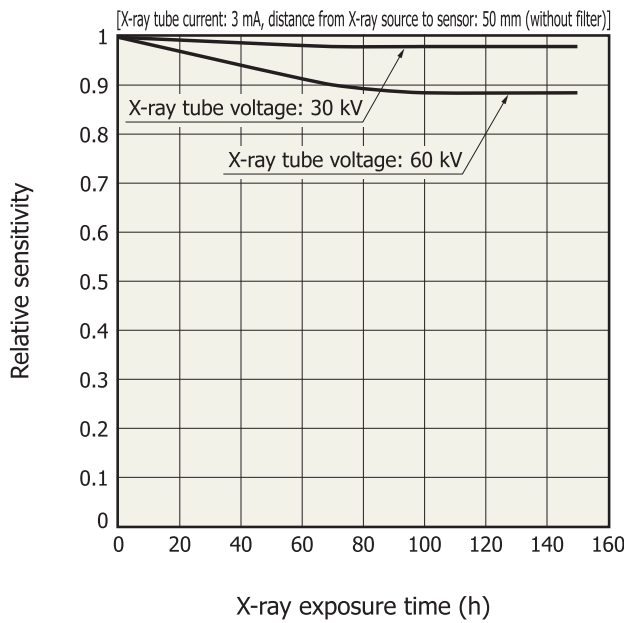
X-ray output example (S8865-64G)



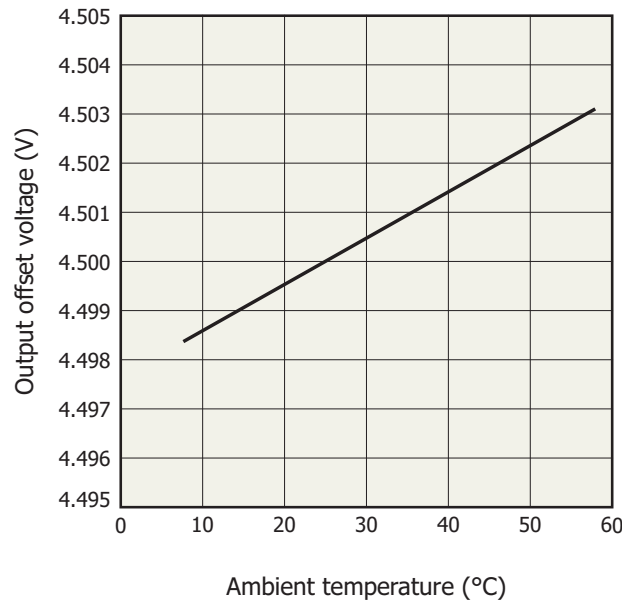
Uniformity example of X-ray output (S8865-64G)



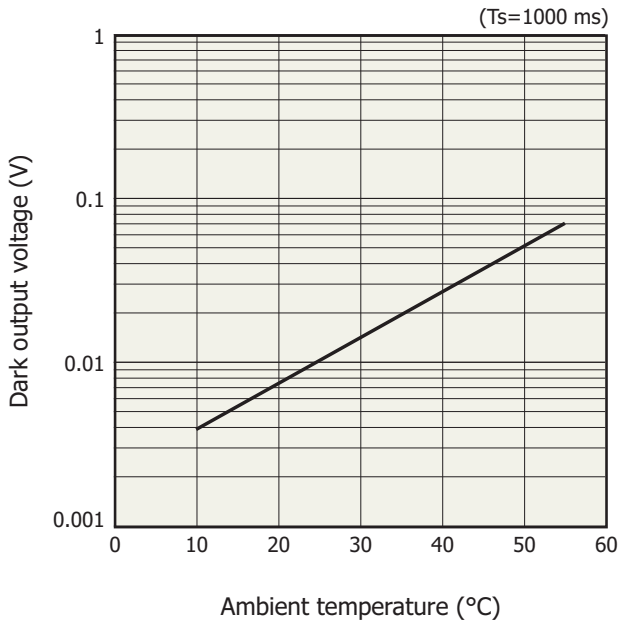
X-ray exposure test example (S8865-128G)



Output offset voltage vs. ambient temperature (measurement example)



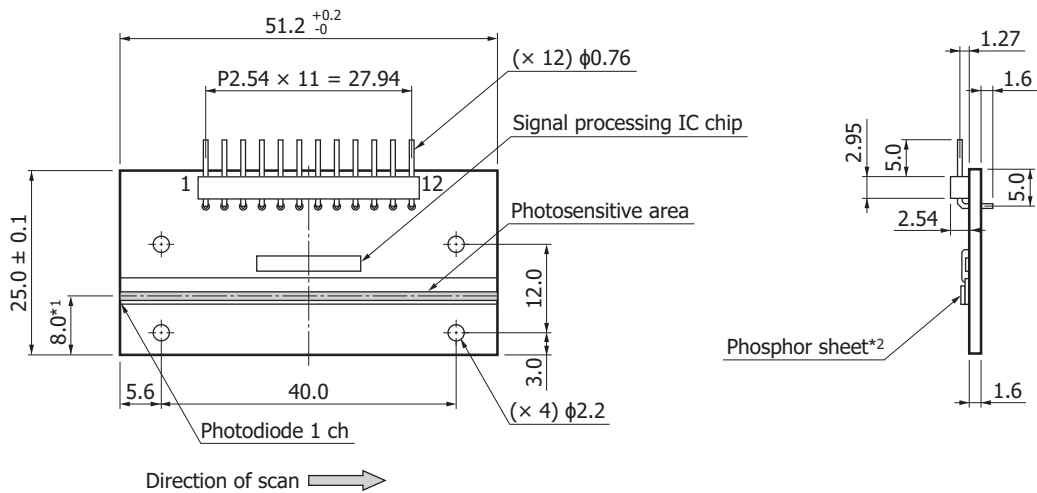
Dark output voltage vs. ambient temperature (measurement example)



KMPDB0289EA

Dimensional outlines (unit: mm)

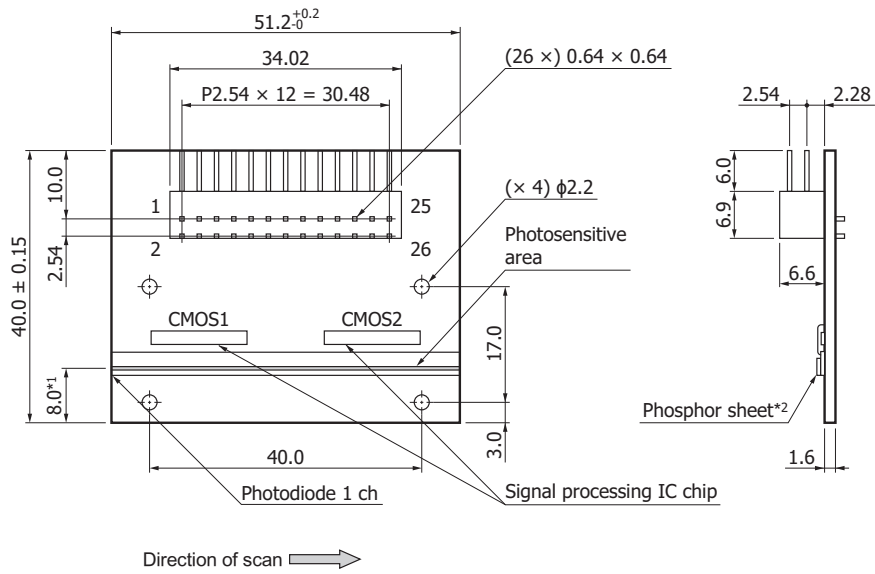
S8865-64G/-128G



- Tolerance unless otherwise noted: ±0.2
- *1: Distance from board bottom to photosensitive area center
Board: G10 glass epoxy
Connector: PRECI-DIP DURTAL 800-10-012-20-001101
 - *2: Photodiode array with phosphor sheet
 - Material: Gd₂O₂S:Tb
 - Phosphor thickness: 300 μm Typ.
 - Detectable energy range: 30 k to 100 keV

KMPDA0292EB

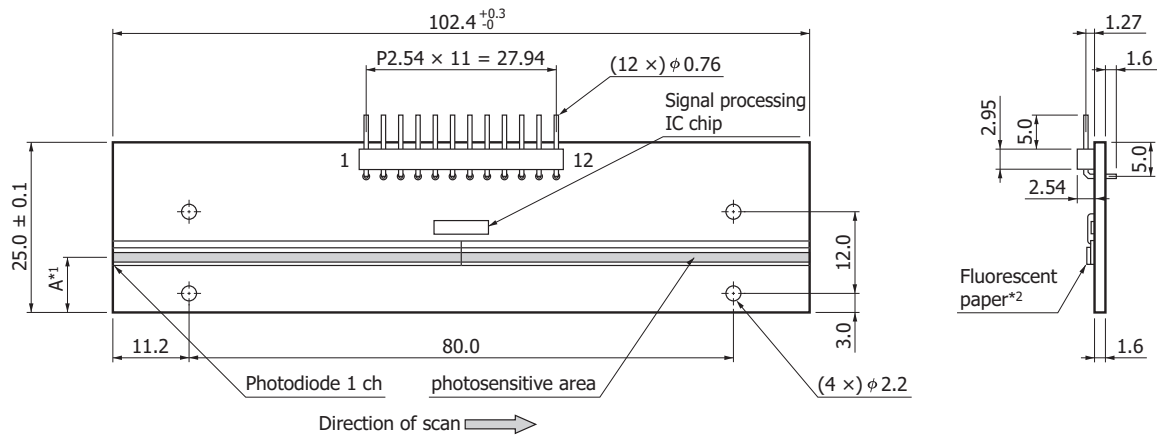
S8865-256G



- Tolerance unless otherwise noted: ± 0.2
- *1: Length from board bottom to photosensitive area center
 - Board: G10 glass epoxy
 - Connector: JAE (Japan Aviation Electronics Industry, Limited)
 - PS-26PE-D4LT1-PN1
 - *2: Photodiode array with phosphor sheet
 - Material: $Gd_2O_2S:Tb$
 - Phosphor thickness: 300 μm typ.
 - Detectable energy range: 30 k to 100 keV

KMPDA0234ED

S8866-64G-02/-128G-02



| Type no. | A |
|-------------|-----|
| S8866-64G2 | 8.2 |
| S8866-128G2 | 8.0 |

- Tolerance unless otherwise noted: ± 0.2
- *1: Length from the bottom of the board to the center of photosensitive area
 - Board: G10 glass epoxy
 - Connector: PRECI-DIP DURTAL 800-10-012-20-001101
 - *2: Photodiode array with phosphor sheet
 - Material: $Gd_2O_2S:Tb$
 - Phosphor thickness: 300 μm typ.
 - Detectable energy range: 30 k to 100 keV

KMPDA0226ED

Pin connection

S8865-64G/-128G, S8866-64G-02/-128G-02

| Pin No. | Symbol | Name | Note |
|---------|--------|---------------------------------------|--|
| 1 | RESET | Reset pulse | Pulse input |
| 2 | CLK | Clock pulse | Pulse input |
| 3 | Trig | Trigger pulse | Positive-going pulse output |
| 4 | EXTSP | External start pulse | Pulse input |
| 5 | Vms | Master/slave selection supply voltage | Voltage input |
| 6 | Vdd | Supply voltage | Voltage input |
| 7 | GND | Ground | |
| 8 | EOS | End of scan | Negative-going pulse output |
| 9 | Video | Video output | Negative-going output with respect to Vref |
| 10 | Vref | Reference voltage | Voltage input |
| 11 | Vgain | Gain selection terminal voltage | Voltage input |
| 12 | Vpd | Photodiode voltage | Voltage input |

S8865-256G

| Pin No. | CMOS1 | Pin No. | CMOS2 | Name | Note |
|---------|-------|---------|-------|---------------------------------------|--|
| 1 | Vpd | 14 | Vpd | Photodiode voltage | Voltage input |
| 2 | RESET | 15 | RESET | Reset pulse | Pulse input |
| 3 | CLK | 16 | CLK | Clock pulse | Pulse input |
| 4 | Trig | 17 | Trig | Trigger pulse | Positive-going pulse output |
| 5 | EXTSP | 18 | EXTSP | External start pulse | Pulse input |
| 6 | Vms | 19 | Vms | Master/slave selection supply voltage | Voltage input |
| 7 | Vdd | 20 | Vdd | Supply voltage | Voltage input |
| 8 | GND | 21 | GND | Ground | |
| 9 | EOS | 22 | EOS | End of scan | Negative-going pulse output |
| 10 | Video | 23 | Video | Video output | Negative-going output with respect to Vref |
| 11 | Vref | 24 | Vref | Reference voltage | Voltage input |
| 12 | Vg | 25 | Vg | Gain selection terminal voltage | Voltage input |
| 13 | Vpd | 26 | Vpd | Photodiode voltage | Voltage input |

Gain selection terminal voltage setting

Vdd: High gain (Cf=0.5 pF) GND: Low gain (Cf=1 pF)

Setting for each readout method

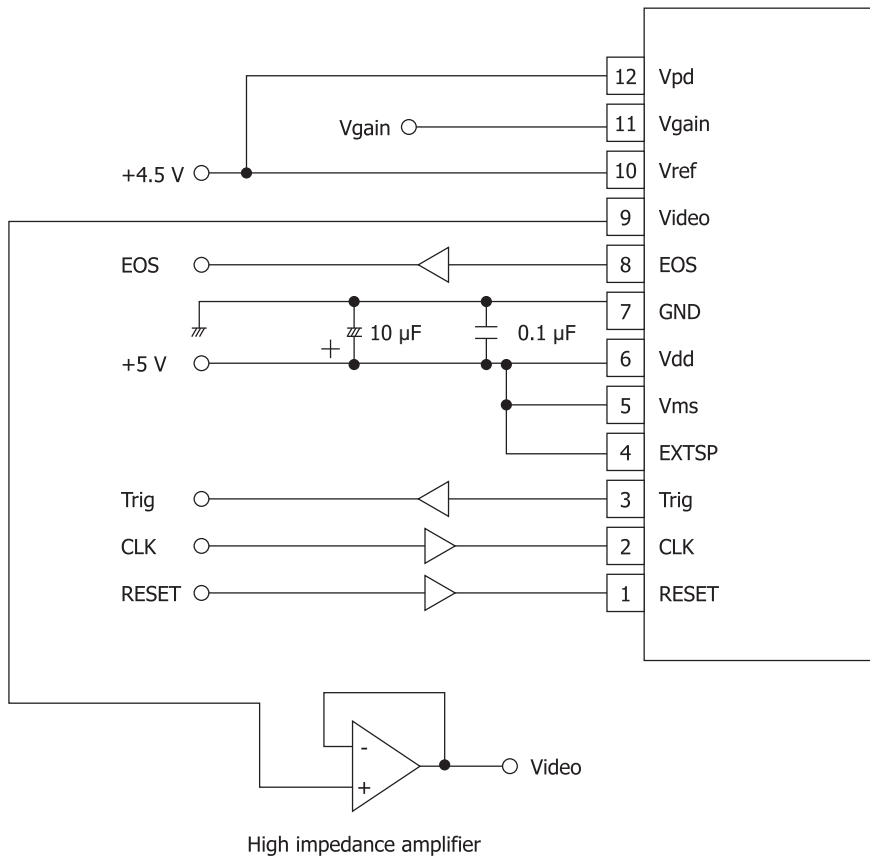
S8866-64G/-128G, S8866-64G-02/-128G-02

Set to A in the table below in most cases.

To serially read out signals from two or more sensors linearly connected, set the 1st sensor to A and the 2nd or later sensors to B. The CLK and RESET pulses should be shared with each sensor and the video output terminal of each sensor connected together.

| Setting | Readout method | Vms | EXTSP |
|---------|--|-----|--------------------------------------|
| A | All stages of parallel readout, serial readout at 1st sensor | Vdd | Vdd |
| B | Serial readout at 2nd and later sensors | GND | Preceding sensor EOS should be input |

[Figure 1] Connection example (parallel readout)



KMPDC0288EB

S8865-256G

Signals of channels 1 through 126 are output from CMOS1, while signals of channels 129 through 256 are output from CMOS2. The following two readout methods are available.

(1) Serial readout method

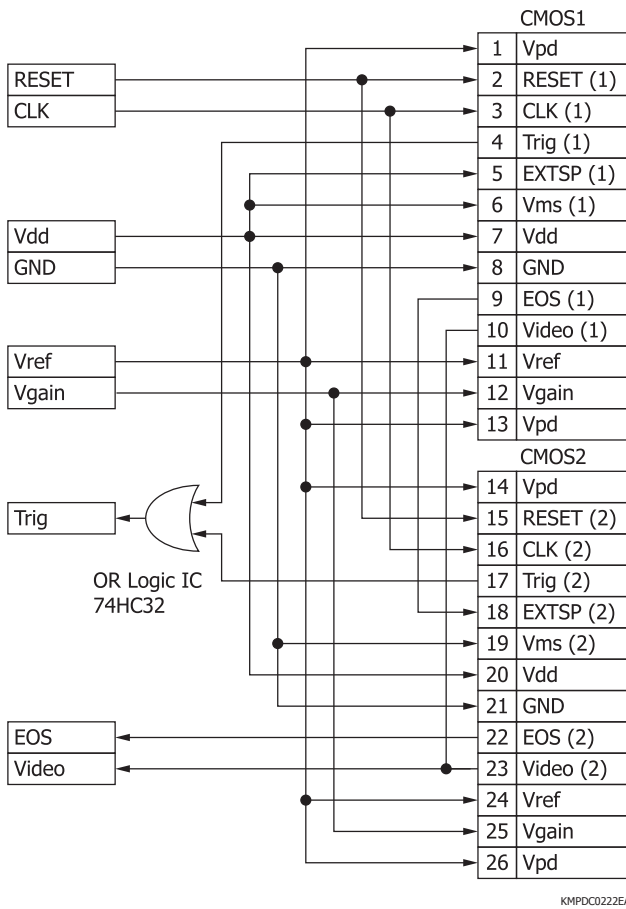
CMOS1 and CMOS2 are connected in serial and the signals of channels 1 through 256 are sequentially read out from one output line. Set CMOS1 as in "A" in the table below, and set CMOS2 as in "B". CMOS1 and CMOS2 should be connected to the same CLK and RESET lines, and their video output terminals to one line.

(2) Parallel readout method

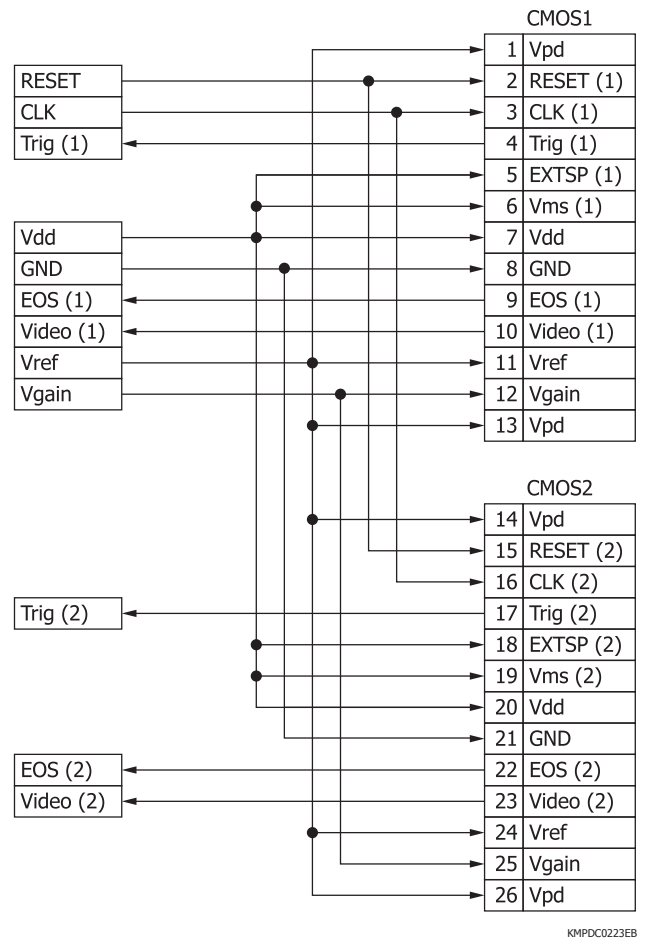
128 channel signals are output in parallel respectively from the output lines of CMOS1 and CMOS2. Set both CMOS1 and CMOS2 as in "A" in the table below.

[Figure 2] Connection

Serial readout method



Parallel readout method



| Setting | Vms | EXTSP |
|---------|-----|--------------------------------------|
| A | Vdd | Vdd |
| B | GND | Preceding sensor EOS should be input |

Readout circuit

Check that pulse signals meet the required pulse conditions before supplying them to the input terminals. Video output should be amplified by an operational amplifier that is connected close to the sensor.

Procautions

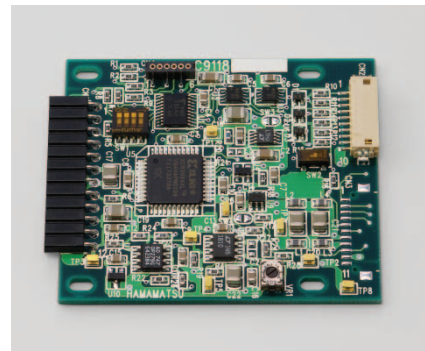
- (1) The signal processing IC chip is protected against static electricity. However, in order to prevent possible damage to the IC chip, take electrostatic countermeasures such as grounding yourself, as well as workbench and tools. Also protect the IC chip from surge voltages from peripheral equipment.
- (2) Gold wires for wire bonding are very thin, so they easily break if subjected to mechanical stress. The signal processing IC chip, wire bonding section and photodiode array chip are covered with resin for protection. However, never touch these portions. Excessive force, if applied, may break the wires or cause malfunction.
Blow air to remove dust or debris if it gets on the protective resin. Never wash them with solvent.
Signals may not be obtained if dust or debris is left or a scratch is made on the protective resin, or the signal processing IC chip or photodiode array chip is nicked.
- (3) The photodiode array characteristics may deteriorate when operated at high humidity, so put it in a hermetically sealed enclosure or case.
When installing the photodiode array on a board, be careful not to cause the board to warp.
- (4) The characteristics of the signal processing IC chip deteriorate if exposed to X-rays. So use a lead shield which is at least 1 mm larger all around than the signal processing IC chip. The 1 mm margin may not be sufficient depending on the incident angle of X-rays. Provide an even larger shield as long as it does not cover the photodiode active area. Since the optimal shield thickness depends on the operating conditions, calculate it by taking the attenuation coefficient of lead into account.
- (5) The sensitivity of the photodiode array chip decreases if continuously exposed to X-rays. The extent of this sensitivity decrease differs depending on the X-ray irradiation conditions, so before beginning measurement, check how much the sensitivity decreases under the X-ray irradiation conditions to be used.

Driver circuit C9118 series (sold separately)

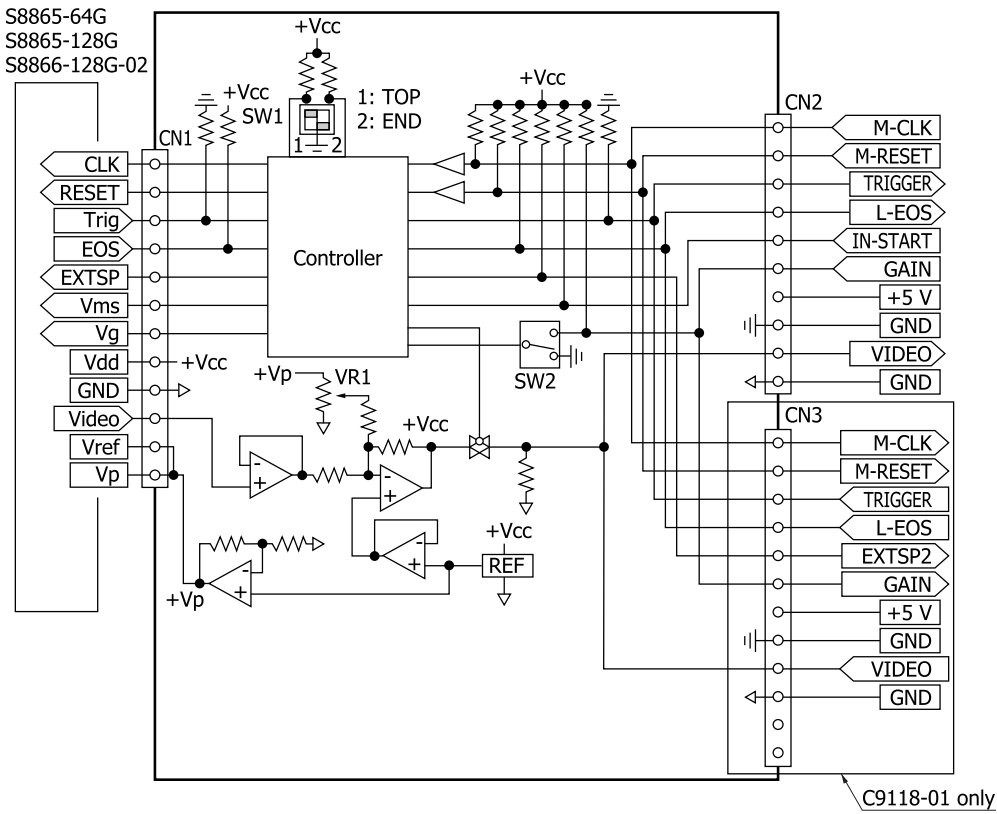
The CMOS driver circuit is designed for the S8865-64G/-128G and S8866-128G-02 photodiode arrays with amplifier. The C9118 series operates a photodiode by just inputting two signals (M-CLK and M-RESET) and a signal +5 V supply. The C9118 is intended for single use or parallel connections, while the C9118-01 is suitable for cascade connections.

Features

- **Single power supply (+5 V) operation**
- **Operation with two input signals (M-CLK and M-RESET)**
- **Compact: 46 × 56 × 5.2^t mm**



Block diagram

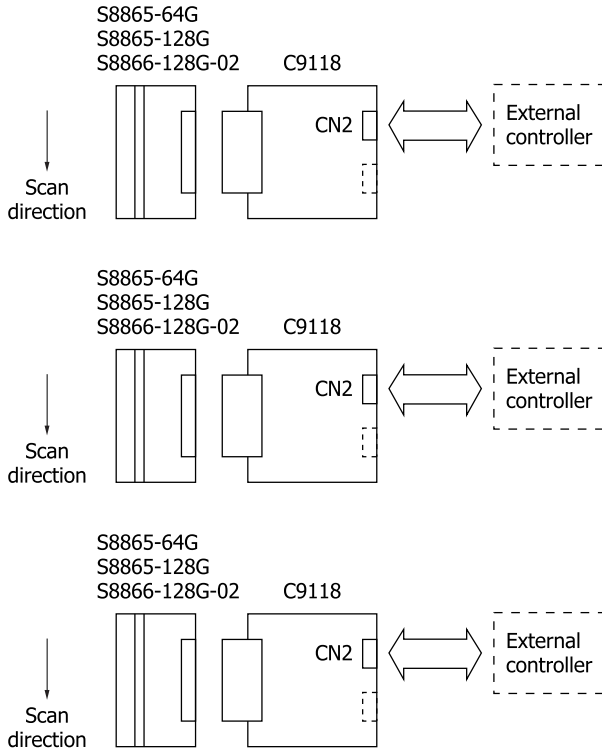


KACCC0455EC

Connection examples

Single or parallel readout example (C9118)

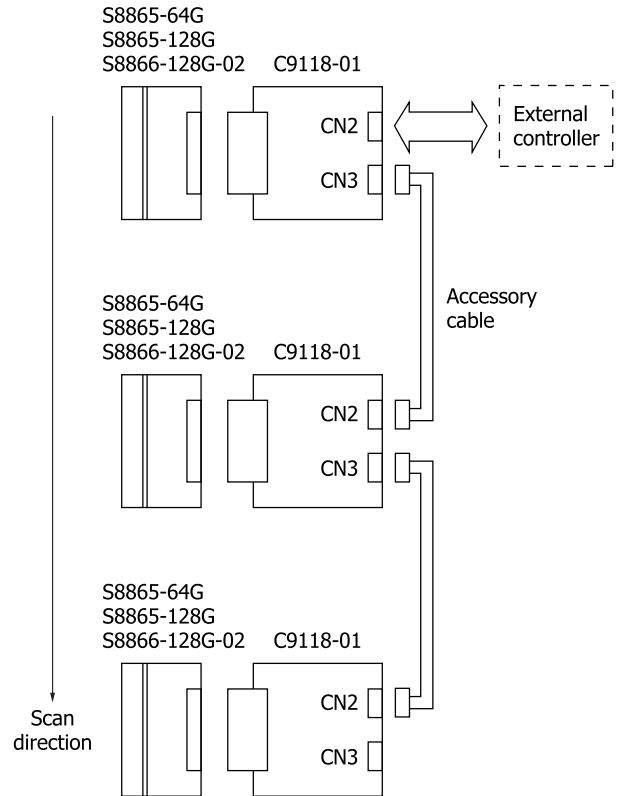
Simultaneous integration/output
(effective for high-speed processing)



KACCC0431EC

Cascade readout example (C9118-01)

Simultaneous integration/serial output
(Simplifies external processing circuit)



KACCC0432EC

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

Precautions

- Disclaimer
- Image sensors

Information described in this material is current as of August 2016.

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HAMAMATSU

www.hamamatsu.com

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 8152-375-0, Fax: (49) 8152-265-8

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39) 02-93581733, Fax: (39) 02-93581741

China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, Beijing 100020, China, Telephone: (86) 10-6586-6006, Fax: (86) 10-6586-2866