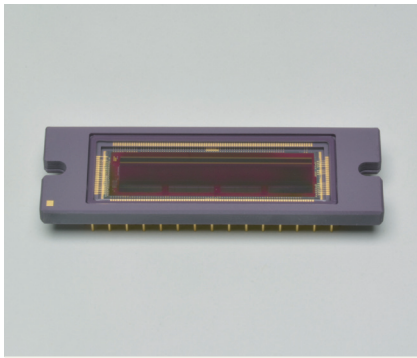


CMOS linear image sensor



S13774

High-speed readout (100 klines/s)

The S13774 is a CMOS linear image sensor developed for industrial cameras that require high-speed scanning. The column-parallel readout system, which has a readout amplifier and an A/D converter for each pixel, allows high-speed readout. For the A/D converter resolution, either 10-bit (high-speed mode: 100 klines/s max.) or 12-bit (low-speed mode: 25 klines/s max.) can be selected. Image data is output serially in 180 MHz LVDS format.

Features

- Pixel size: 7 × 7 μm
- Number of pixels: 4096
- High-speed readout: 100 klines/s
- Simultaneous integration of all pixels
- 3.3 V power supply operation
- SPI communication function
- Built-in 10-bit/12-bit A/D converters

Applications

- Machine vision
- Film inspection
- Printed circuit board appearance inspection
- Print inspection

Structure

| Parameter | Specification | Unit |
|--------------------------------------|-------------------------------|------|
| Number of pixels | 4096 | - |
| Pixel pitch | 7 | μm |
| Pixel height | 7 | μm |
| Effective photosensitive area length | 28.672 | mm |
| Package | Ceramic | - |
| Window material*1 | Borosilicate glass (D263Teco) | - |

*1: AR coated (1% or less reflectance at 400 to 800 nm)

Absolute maximum ratings (Ta=25 °C)

| Parameter | Symbol | Condition | Value | Unit |
|---|------------------|-----------------------|--------------|------|
| Supply voltage | Analog terminal | Vdd(A) | -0.3 to +3.9 | V |
| | Digital terminal | Vdd(D) | -0.3 to +3.9 | V |
| | Counter terminal | Vdd(C) | -0.3 to +3.9 | V |
| Digital input signal terminal voltage*2 | Vi | | -0.3 to +3.9 | V |
| Vref_cp1 terminal voltage | Vref_cp1 | | -0.3 to +6.5 | V |
| Vref_cp2 terminal voltage | Vref_cp2 | | -2.0 to +0.3 | V |
| Operating temperature | Topr | No dew condensation*3 | -5 to +70 | °C |
| Storage temperature | Tstg | No dew condensation*3 | -10 to +70 | °C |

*2: CS, SCLK, MOSI, RSTB, MCLK, MST, All-reset, Pll-reset

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|-----------------------|------------------|--------|------|--------|---------------|---|
| Supply voltage | Analog terminal | Vdd(A) | 3.15 | 3.3 | 3.45 | V |
| | Digital terminal | Vdd(D) | 3.15 | 3.3 | 3.45 | |
| | Counter terminal | Vdd(C) | 3.15 | 3.3 | 3.45 | |
| Digital input voltage | High level | Vi(H) | 3 | Vdd(D) | Vdd(D) + 0.25 | V |
| | Low level | Vi(L) | 0 | - | 0.3 | |

Electrical characteristics

■ Digital input signal [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, unless otherwise noted]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------|----------|------|------|------|------|
| Master clock pulse frequency | f(MCLK) | 29 | 30 | 31 | MHz |
| Master clock pulse duty cycle | D(MCLK) | 45 | 50 | 55 | % |
| Rise time*4 | tr(sigi) | - | 5 | 7 | ns |
| Fall time*4 | tf(sigi) | - | 5 | 7 | ns |

*4: Time for the input voltage to rise or fall between 10% and 90%

■ Digital output signal [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=30 MHz, unless otherwise noted]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------|-----------------|-------------|--------|------|----------|
| Video data rate (LVDS) | DR | f(MCLK)×6 | | | MHz |
| Line rate | High-speed mode | - | - | 100 | klines/s |
| | Low-speed mode | - | - | 25 | |
| LVDS output voltage*5 | Offset | 1.13 | 1.25 | 1.38 | V |
| | Differential | 0.25 | 0.35 | 0.45 | |
| LVDS rise time*6 | tr(LVDS) | - | 2 | 3 | ns |
| LVDS fall time*6 | tf(LVDS) | - | 2 | 3 | ns |
| CMOS output voltage | High | Vdd(D)-0.25 | Vdd(D) | - | V |
| | Low | - | 0 | 0.25 | |
| CMOS output rise time*7 | tr(sigo) | - | 10 | 12 | ns |
| CMOS output fall time*7 | tf(sigo) | - | 10 | 12 | ns |

*5: Attach a 100 Ω terminator to the LVDS output terminal.

*6: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal

*7: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal

■ Current consumption [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=30 MHz, LR=100 klines/s, unless otherwise noted]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------|--------|------|------|------|------|
| Vdd(A) terminal*8 | Ic1 | 80 | 140 | 200 | mA |
| Vdd(D) terminal*8 | Ic2 | 220 | 400 | 530 | |
| Vdd(C) terminal*8 | Ic3 | 510 | 810 | 1110 | |

*8: Apply saturation exposure light.

Electrical characteristics of A/D converter [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=30 MHz, unless otherwise noted]

| Parameter | Symbol | Specification | Unit |
|--------------------------|-----------------|---------------|------|
| Resolution | High-speed mode | 10*9 | bit |
| | Low-speed mode | 12 | |
| Conversion voltage range | - | 0 to 1.3 | V |

*9: Equivalent to 10-bit. From offset output to saturated output is approximately 1024 DN.

■ Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V, f(MCLK)=30 MHz, gain: default value, offset: default value, tpi(MST)=10 μs (high-speed mode), 40 μs (low-speed mode), unless otherwise noted]

■ Common to all modes

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------|-------------|-------------|------|------|-----------------|
| Spectral response range | λ | 400 to 1000 | | | nm |
| Peak sensitivity wavelength | λ_p | - | 700 | - | nm |
| Photoresponse nonuniformity*10 | Gain 1 | PRNU | ±5 | ±10 | % |
| | Gain 8 | | ±5 | ±10 | |
| Image lag*11 | Lag | - | - | 0.1 | % |
| Saturation charge | Qsat | 29 | 30 | - | ke ⁻ |
| SNR max. | Gain 1 | - | 43 | 45 | dB |
| | Gain 8 | | 32 | 35 | |

*10: The output uniformity when a uniform light with a light exposure that is approximately 50% of saturation output is applied. It is defined as follows for the 4090 pixels excluding the 3 pixels at each end of the sensor.

$$PRNU = (\Delta X/X) \times 100 [\%]$$

*11: The signal component of the previous data that remains after data is read out under saturation output conditions. Image lag increases if light greater than the saturation exposure is incident.

■ High-speed mode

| Parameter | Symbol | Gain | Min. | Typ. | Max. | Unit |
|-----------------------|--------|------|------|------|------|--------------------|
| Offset variation*12 | VSNU | 1 | - | 3 | 18 | mV |
| | | | - | 2.4 | 14.4 | DN |
| | | 8 | - | 7.5 | 45 | mV |
| | | | - | 6 | 36 | DN |
| Dark output*13 | VD | 1 | - | 0.5 | 20 | mV |
| | | | - | 0.4 | 16 | DN |
| | | 8 | - | 4 | 160 | mV |
| | | | - | 3.2 | 128 | DN |
| Photosensitivity*14 | Sw | 1 | - | 45 | - | V/(lx·s) |
| | | | - | 36k | - | DN/(lx·s) |
| | | 8 | - | 360 | - | V/(lx·s) |
| | | | - | 290k | - | DN/(lx·s) |
| Conversion efficiency | CE | 1 | - | 42 | - | μV/e ⁻ |
| | | | - | 33 | - | mDN/e ⁻ |
| | | 8 | - | 340 | - | μV/e ⁻ |
| | | | - | 270 | - | mDN/e ⁻ |
| Saturation output | Vsat | - | 1.2 | 1.25 | - | V |
| | | | 975 | 1000 | - | DN |
| Readout noise*15 | Nread | 1 | - | 0.63 | 1.9 | mV-rms |
| | | | - | 0.5 | 1.5 | DN-rms |
| | | 8 | - | 1.5 | 4.5 | mV-rms |
| | | | - | 1.2 | 3.6 | DN-rms |
| Dynamic range*16 | Drange | 1 | 670 | 2000 | - | - |
| | | 8 | 260 | 800 | - | - |

■ Low-speed mode

| Parameter | Symbol | Gain | Min. | Typ. | Max. | Unit |
|-----------------------|--------|------|------|-------|------|-------------------|
| Offset variation*12 | VSNU | 1 | - | 3 | 18 | mV |
| | | | - | 9.6 | 57.6 | DN |
| | | 8 | - | 7.5 | 45 | mV |
| | | | - | 24 | 144 | DN |
| Dark output*13 | VD | 1 | - | 0.5 | 20 | mV |
| | | | - | 1.6 | 64 | DN |
| | | 8 | - | 4 | 160 | mV |
| | | | - | 12.8 | 512 | DN |
| Photosensitivity*14 | Sw | 1 | - | 45 | - | V/(lx·s) |
| | | | - | 140k | - | DN/(lx·s) |
| | | 8 | - | 360 | - | V/(lx·s) |
| | | | - | 1200k | - | DN/(lx·s) |
| Conversion efficiency | CE | 1 | - | 42 | - | $\mu\text{V}/e^-$ |
| | | | - | 130 | - | mDN/ e^- |
| | | 8 | - | 340 | - | $\mu\text{V}/e^-$ |
| | | | - | 1100 | - | mDN/ e^- |
| Saturation output | Vsat | - | 1.2 | 1.25 | - | V |
| | | - | 3900 | 4000 | - | DN |
| Readout noise*15 | Nread | 1 | - | 0.38 | 1.1 | mV-rms |
| | | | - | 1.2 | 3.6 | DN-rms |
| | | 8 | - | 1.6 | 4.7 | mV-rms |
| | | | - | 5 | 15 | DN-rms |
| Dynamic range*16 | Drange | 1 | 1100 | 3300 | - | - |
| | | 8 | 260 | 800 | - | - |

*12: Measured in the dark state. Difference between the maximum and minimum.

*13: $T_s=10$ ms, voltage difference from the offset output level

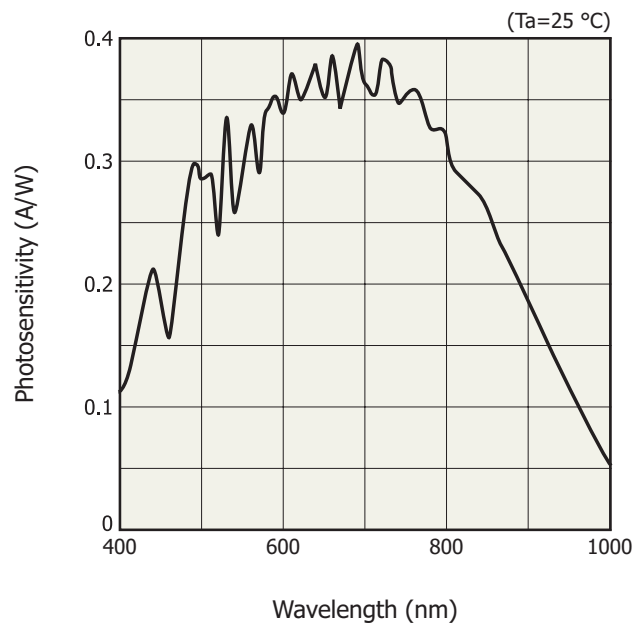
*14: 2856 K, tungsten lamp

*15: Dark state

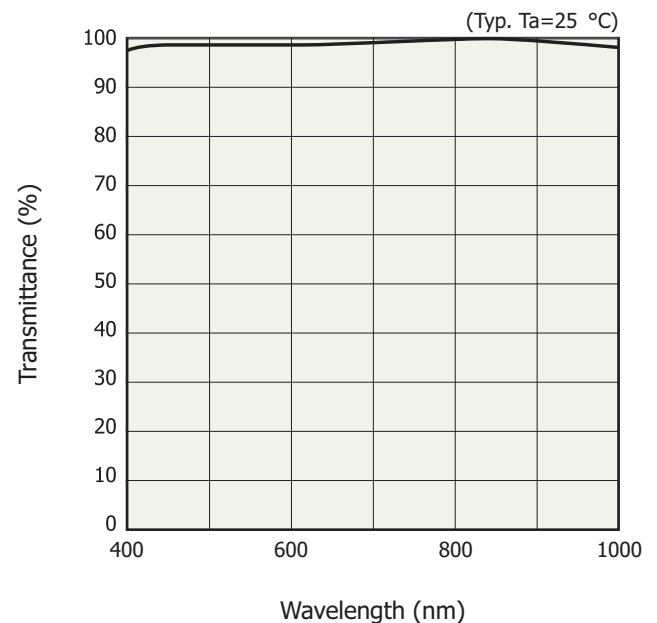
*16: V_{sat}/N_{read}

Note: DN (digital number): unit of A/D converter output

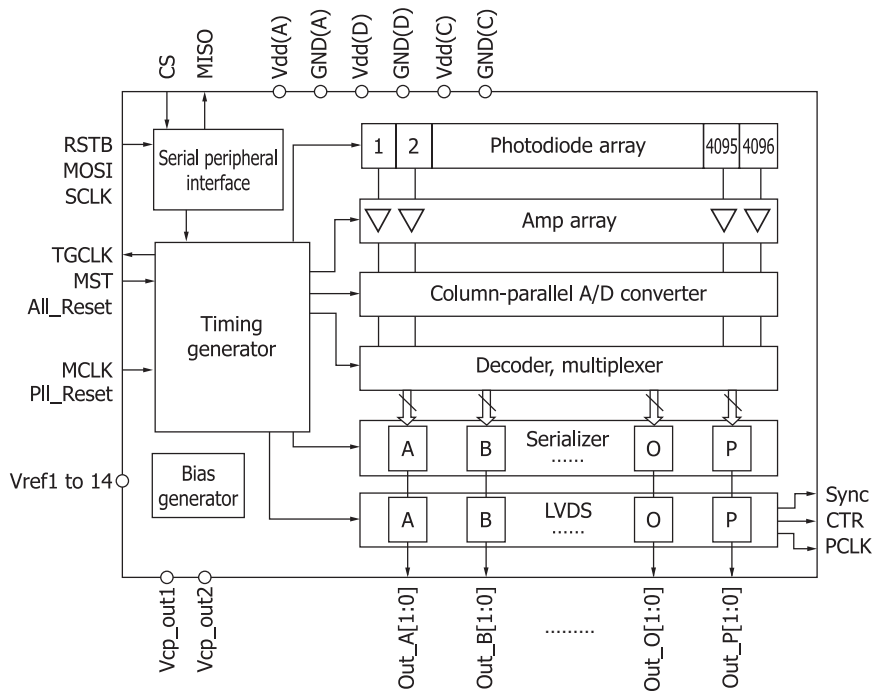
■ Spectral response (typical example)



■ Spectral transmittance characteristics of window material



Block diagram



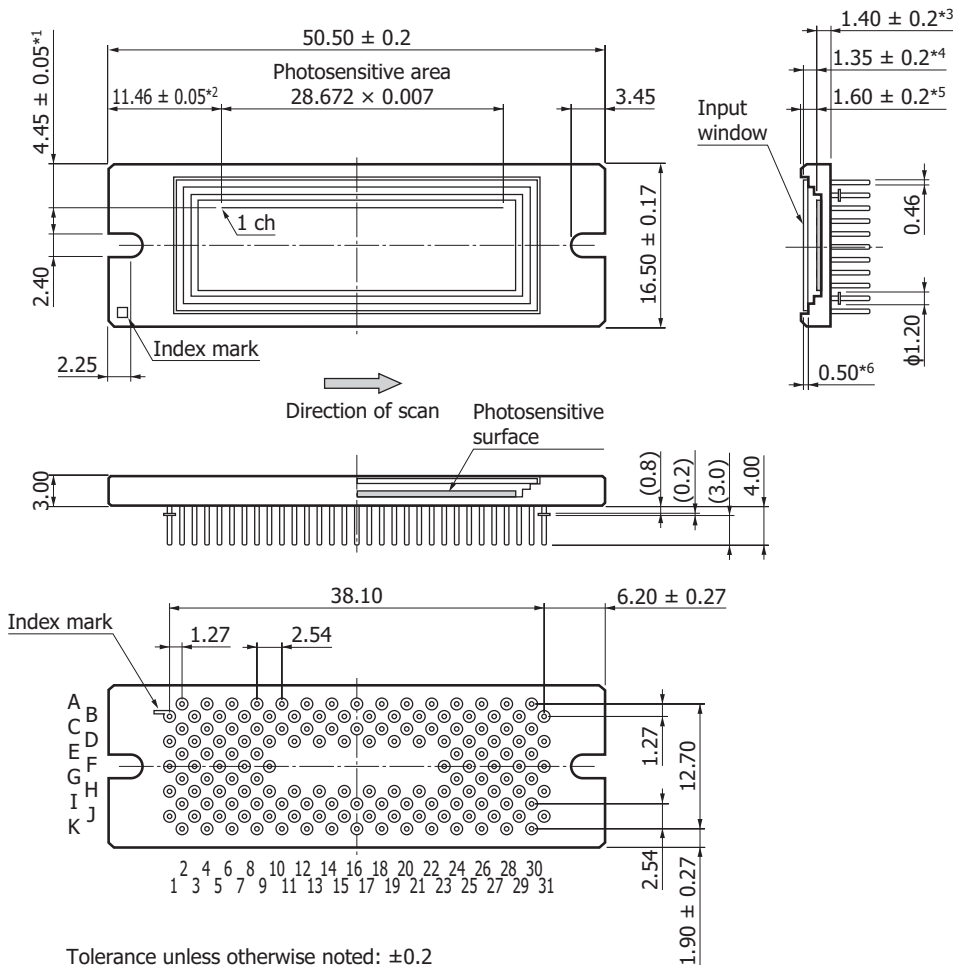
KMPDC0637EA

Setup using the SPI and the like

The following parameters can be set using the SPI (serial peripheral interface).

| Parameter | Mode and explanation | |
|----------------------------------|---|---|
| High-speed mode | The maximum line rate is 100 kline/s. The A/D converter resolution is 10-bit. (From offset output to saturated output is approximately 1024 DN.) | |
| Low-speed mode | The maximum line rate is 25 kline/s. The A/D converter resolution is 12-bit. | |
| Number of video output terminals | Full output mode | Output from 64 terminals (32 LVDS pairs). |
| | 1/4 output mode | Output from 16 terminals (8 LVDS pairs). Do not use this setting if the line rate is to be shorter than 25 klines/s. |
| Output gain | The default gain is 1x. It can be set to any of the six settings: 1, 2, 4, 8, 10, 20. | |
| Output offset | The output offset value can be set between 0 DN to 1023 DN (1024 steps). | |

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ± 0.2

- *1: Distance from package edge to photosensitive area center
- *2: Distance from package edge to 1 ch edge
- *3: Distance from package bottom to photosensitive area
- *4: Distance from glass surface to photosensitive surface
- *5: Distance from package top to photosensitive surface
- *6: Glass thickness

KMPDA0572EA

Pin connections

| Pin no. | Symbol | Function | I/O | Pin no. | Symbol | Function | I/O |
|---------|-----------|--|-----|---------|-----------|-------------------------------|-----|
| A2 | Out_An[0] | Video output signal | O | D23 | Vref6 | Bias voltage*17 | O |
| A4 | Out_An[1] | Video output signal | O | D25 | Syncp | Frame sync signal | O |
| A6 | Out_Cn[0] | Video output signal | O | D27 | MST | Master start signal | I |
| A8 | Out_Cn[1] | Video output signal | O | D29 | GND(C) | Ground | - |
| A10 | Out_En[0] | Video output signal | O | D31 | Vdd(C) | Supply voltage (3.3 V) | I |
| A12 | Out_En[1] | Video output signal | O | E2 | Vdd(D) | Supply voltage (3.3 V) | I |
| A14 | Out_Gn[0] | Video output signal | O | E4 | GND | Ground | - |
| A16 | Out_Gn[1] | Video output signal | O | E6 | PII_Reset | PII circuit reset | I |
| A18 | Out_In[0] | Video output signal | O | E8 | CS | SPI selection signal | I |
| A20 | Out_In[1] | Video output signal | O | E24 | NC | No connection | - |
| A22 | Out_Kn[0] | Video output signal | O | E26 | All_Reset | Timing generator reset | I |
| A24 | Out_Kn[1] | Video output signal | O | E28 | GND(C) | Ground | - |
| A26 | Out_Mn[0] | Video output signal | O | E30 | Vdd(C) | Supply voltage (3.3 V) | I |
| A28 | Out_Mn[1] | Video output signal | O | F1 | Vdd(D) | Supply voltage (3.3 V) | I |
| A30 | Out_On[0] | Video output signal | O | F3 | GND | Ground | - |
| B1 | Out_Ap[0] | Video output signal | O | F5 | SCLK | SPI clock signal | I |
| B3 | Out_Ap[1] | Video output signal | O | F7 | MOSI | SPI input signal | I |
| B5 | Out_Cp[0] | Video output signal | O | F9 | RSTB | SPI reset signal | I |
| B7 | Out_Cp[1] | Video output signal | O | F23 | NC | No connection | - |
| B9 | Out_Ep[0] | Video output signal | O | F25 | NC | No connection | - |
| B11 | Out_Ep[1] | Video output signal | O | F27 | NC | No connection | - |
| B13 | Out_Gp[0] | Video output signal | O | F29 | GND(C) | Ground | - |
| B15 | Out_Gp[1] | Video output signal | O | F31 | Vdd(C) | Supply voltage (3.3 V) | I |
| B17 | Out_Ip[0] | Video output signal | O | G2 | Vdd(D) | Supply voltage (3.3 V) | I |
| B19 | Out_Ip[1] | Video output signal | O | G4 | GND | Ground | - |
| B21 | Out_Kp[0] | Video output signal | O | G6 | MISO | SPI output signal | O |
| B23 | Out_Kp[1] | Video output signal | O | G8 | TGCLK | Timing generator clock signal | O |
| B25 | Out_Mp[0] | Video output signal | O | G24 | NC | No connection | - |
| B27 | Out_Mp[1] | Video output signal | O | G26 | NC | No connection | - |
| B29 | Out_Op[0] | Video output signal | O | G28 | GND(C) | Ground | - |
| B31 | Out_Op[1] | Video output signal | O | G30 | Vdd(C) | Supply voltage (3.3 V) | I |
| C2 | Vdd(D) | Supply voltage (3.3 V) | I | H1 | Vdd(D) | Supply voltage (3.3 V) | I |
| C4 | GND | Ground | - | H3 | GND | Ground | - |
| C6 | PCLKn | Bit output sync signal | O | H5 | NC | No connection | - |
| C8 | CTRn | Pixel sync signal | O | H7 | NC | No connection | - |
| C10 | NC | No connection | - | H9 | Vref7 | Bias voltage*17 | O |
| C12 | NC | No connection | - | H11 | Vref8 | Bias voltage*17 | O |
| C14 | NC | No connection | - | H13 | Vref9 | Bias voltage*17 | O |
| C16 | NC | No connection | - | H15 | Vref10 | Bias voltage*17 | O |
| C18 | NC | No connection | - | H17 | Vref11 | Bias voltage*17 | O |
| C20 | NC | No connection | - | H19 | Vref12 | Bias voltage*17 | O |
| C22 | NC | No connection | - | H21 | Vref13 | Bias voltage*17 | O |
| C24 | NC | No connection | - | H23 | Vref14 | Bias voltage*17 | O |
| C26 | Syncn | Frame sync signal | O | H25 | NC | No connection | - |
| C28 | MCLK | Master clock signal | I | H27 | NC | No connection | - |
| C30 | Out_On[1] | Video output signal | O | H29 | GND(C) | Ground | - |
| D1 | Vdd(D) | Supply voltage (3.3 V) | I | H31 | Vdd(C) | Supply voltage (3.3 V) | I |
| D3 | GND | Ground | - | I2 | Vdd(D) | Supply voltage (3.3 V) | I |
| D5 | PCLKp | Bit output sync signal | O | I4 | GND | Ground | - |
| D7 | CTRp | Pixel sync signal | O | I6 | NC | No connection | - |
| D9 | Vref_cp1 | Bias voltage for charge pump circuit (5.5 V)*17 | O | I8 | NC | No connection | - |
| D11 | Vref_cp2 | Bias voltage for charge pump circuit (-1.5 V)*17 | O | I10 | Vdd(A) | Supply voltage (3.3 V) | I |
| D13 | Vref1 | Bias voltage*17 | O | I12 | GND | Ground | - |
| D15 | Vref2 | Bias voltage*17 | O | I14 | Vdd(A) | Supply voltage (3.3 V) | I |
| D17 | Vref3 | Bias voltage*17 | O | I16 | GND | Ground | - |
| D19 | Vref4 | Bias voltage*17 | O | I18 | Vdd(A) | Supply voltage (3.3 V) | I |
| D21 | Vref5 | Bias voltage*17 | O | I20 | GND | Ground | - |

*17: Insert a 1 μ F capacitor between each terminal and GND.
 Note: Leave NC pins open; do not connect to GND.

| Pin no. | Symbol | Function | I/O | Pin no. | Symbol | Function | I/O |
|---------|-----------|------------------------|-----|---------|-----------|---------------------|-----|
| I22 | Vdd(A) | Supply voltage (3.3 V) | I | J27 | Out_Np[1] | Video output signal | O |
| I24 | GND | Ground | - | J29 | Out_Pp[0] | Video output signal | O |
| I26 | NC | No connection | - | J31 | Out_Pn[1] | Video output signal | O |
| I28 | NC | No connection | - | K2 | Out_Bn[0] | Video output signal | O |
| I30 | Out_Pn[1] | Video output signal | O | K4 | Out_Bn[1] | Video output signal | O |
| J1 | Out_Bp[0] | Video output signal | O | K6 | Out_Dn[0] | Video output signal | O |
| J3 | Out_Bp[1] | Video output signal | O | K8 | Out_Dn[1] | Video output signal | O |
| J5 | Out_Dp[0] | Video output signal | O | K10 | Out_Fn[0] | Video output signal | O |
| J7 | Out_Dp[1] | Video output signal | O | K12 | Out_Fn[1] | Video output signal | O |
| J9 | Out_Fp[0] | Video output signal | O | K14 | Out_Hn[0] | Video output signal | O |
| J11 | Out_Fp[1] | Video output signal | O | K16 | Out_Hn[1] | Video output signal | O |
| J13 | Out_Hp[0] | Video output signal | O | K18 | Out_Jn[0] | Video output signal | O |
| J15 | Out_Hp[1] | Video output signal | O | K20 | Out_Jn[1] | Video output signal | O |
| J17 | Out_Jp[0] | Video output signal | O | K22 | Out_Ln[0] | Video output signal | O |
| J19 | Out_Jp[1] | Video output signal | O | K24 | Out_Ln[1] | Video output signal | O |
| J21 | Out_Lp[0] | Video output signal | O | K26 | Out_Nn[0] | Video output signal | O |
| J23 | Out_Lp[1] | Video output signal | O | K28 | Out_Nn[1] | Video output signal | O |
| J25 | Out_Np[0] | Video output signal | O | K30 | Out_Pn[0] | Video output signal | O |

Note: The video output symbol is defined as follows:

Out_An[0]

[0]: lower (0 to 5) bits, [1]: higher (6 to 11) bits

p: positive input of the differential pair, n: negative input of the differential pair

A to P: output ports

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window

If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Operating and storage environments

Handle the device within the temperature range of the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

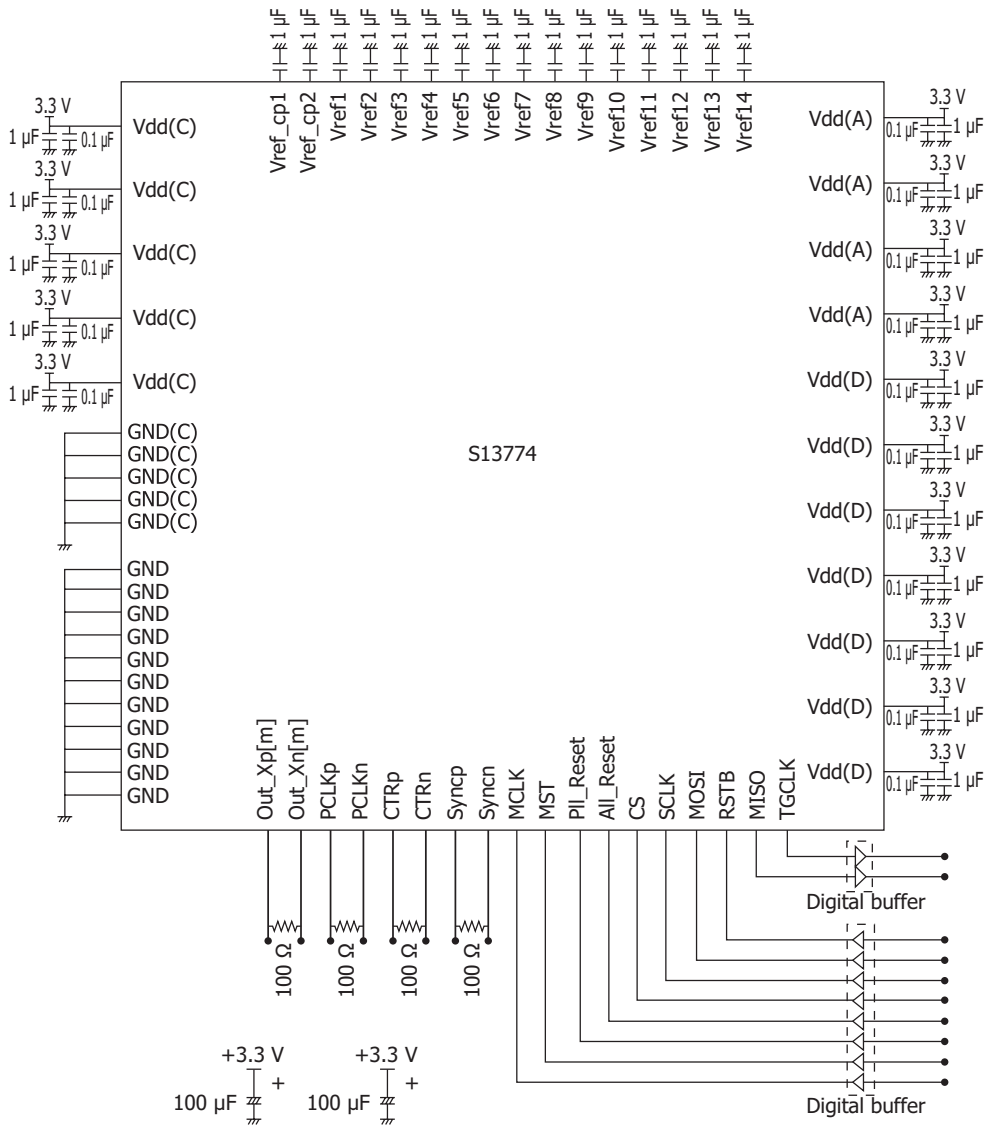
(5) UV light irradiation

Because this product is not designed to resist characteristic deterioration under UV light irradiation, do not apply UV light irradiation to it.

(6) Fixing the product in place

When using screws to fix the product in place, use M2 screws. Set the tightening torque to 0.08 N·m or less.

Connection circuit example



Ground GND and GND(C) to a single point.

KMPDC0638EA

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

- Precautions
- Disclaimer
- Image sensors

Information described in this material is current as of January 2018.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

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